2M x 32 SDRAM

512K x 32bit x 4 Banks Synchronous DRAM LVTTL

Revision 1.1

November 1999

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Revision History

Revision 1.1 (November 17th, 1999)

- Corrected typo in ordering information on page 3

Revision 1.0 (October, 1999)

- Changed part number from KM432S2030CT-G/F to K4S643232C-TC/TL according to re-organized code system

512K x 32Bit x 4 Banks Synchronous DRAM

FEATURES

- 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 15.6us refresh duty cycle

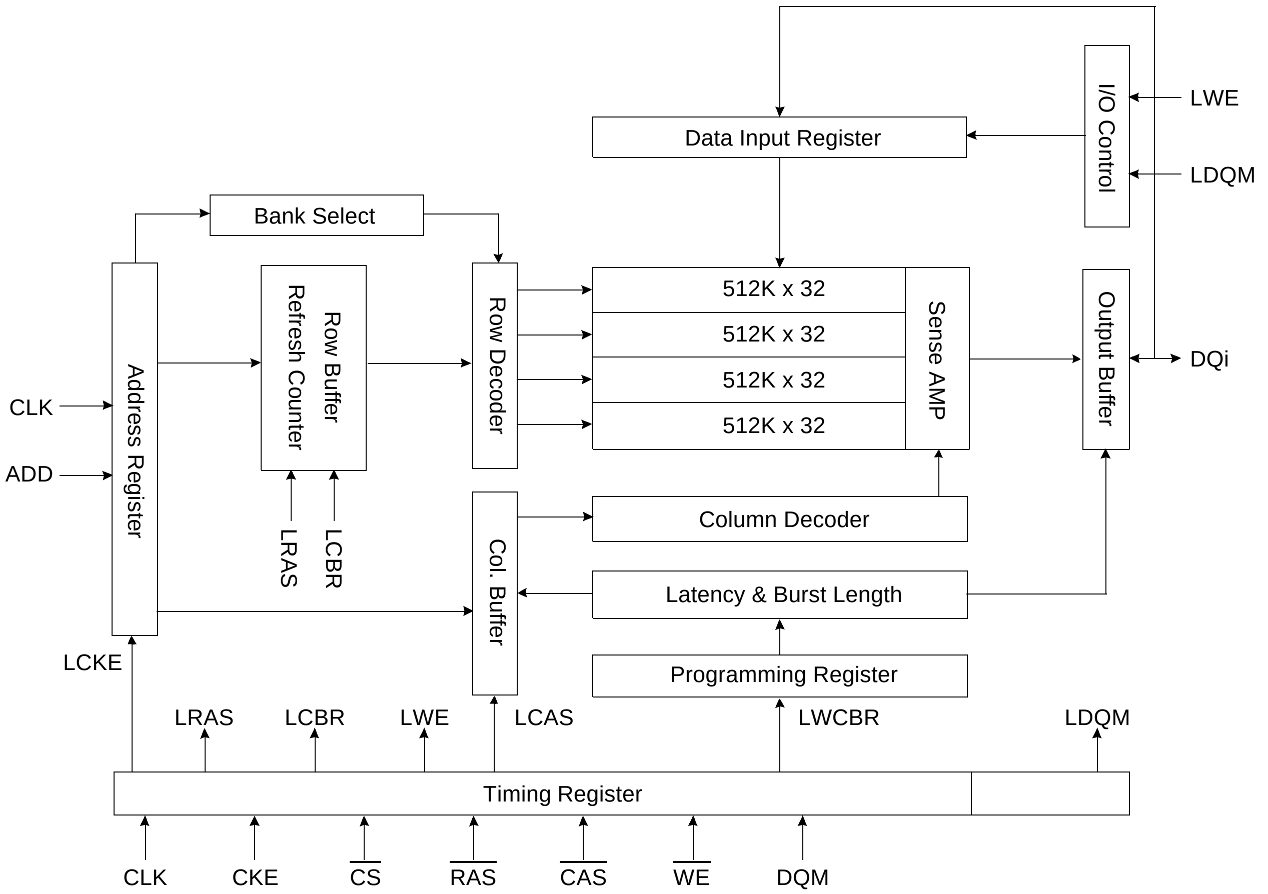
GENERAL DESCRIPTION

The K4S643232C is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 524,288 words by 32 bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

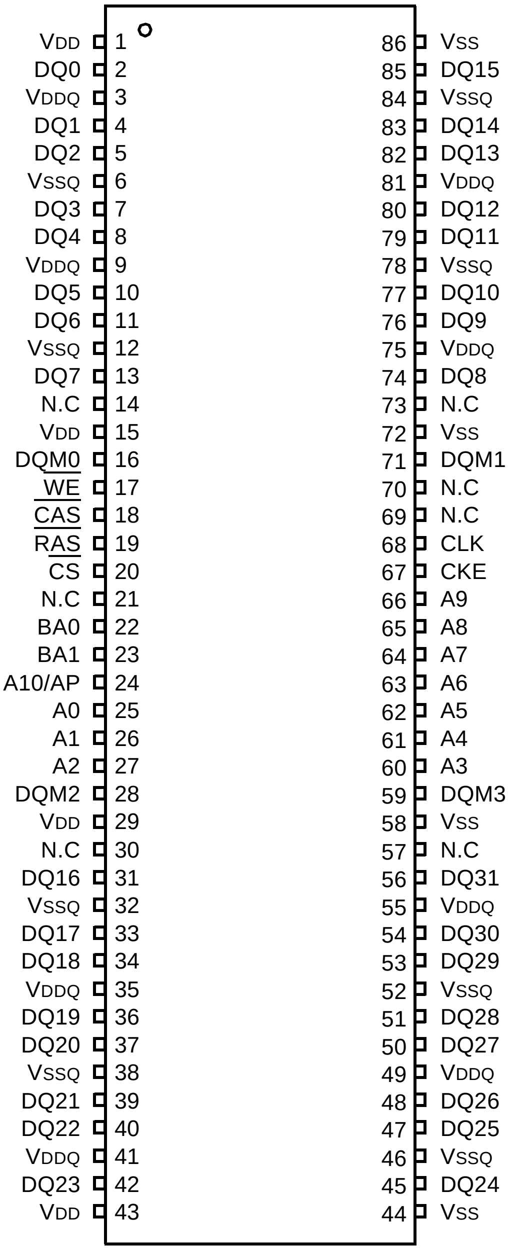
Part NO.	Max Freq.	Interface	Package
K4S643232C-TC/L55	183MHz		
K4S643232C-TC/L60	166MHz		
K4S643232C-TC/L70	143MHz	LVTTL	86 TSOP(II)
K4S643232C-TC/L80	125MHz		
K4S643232C-TC/L10	100MHz		

FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION (Top view)



86Pin TSOP (II)
(400mil x 875mil)
(0.5 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power down mode.
A_0 ~ A_{10}	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{10}, Column address : CA_0 ~ CA_7
BA0,1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 3	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
DQ_0 ~ $_{31}$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	*No Connection*	This pin is recommended to be left No connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Clock	C_{CLK}	2.5	4	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	C_{IN}	2.5	4.5	pF
Address	C_{ADD}	2.5	4.5	pF
DQ_0 ~ DQ_{31}	C_{OUT}	4.0	6.5	pF

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	4
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ},
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. The VDD condition of K4S643232C-55/60 is 3.135V~3.6V.

DC CHARACTERISTICS

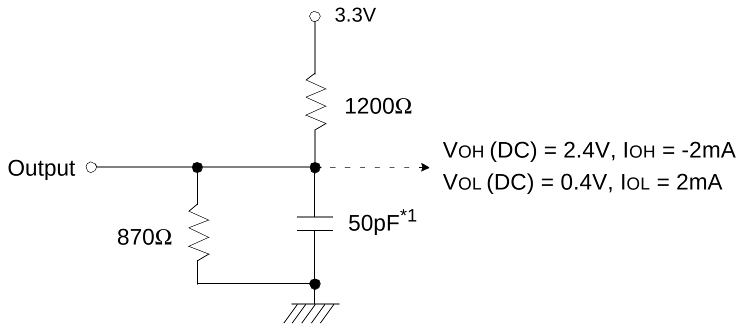
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Test Condition</th><th rowspan="2">CAS Latency</th><th colspan="5">Version</th><th rowspan="2">Unit</th><th rowspan="2">Note</th></tr>
<tr><th>-55</th><th>-60</th><th>-70</th><th>-80</th><th>-10</th></tr>
<tr><td rowspan="2">Operating current
(One bank active)</td><td rowspan="2">I_{CC1}</td><td rowspan="2">Burst length = 1
t_{RC} ≥ t_{RC}(min)
I_o = 0 mA</td><td>3</td><td>140</td><td>140</td><td>130</td><td>130</td><td>115</td><td rowspan="2">mA</td><td rowspan="2">2</td></tr>
<tr><td>2</td><td>-</td><td>-</td><td>-</td><td>130</td><td>115</td></tr>
<tr><td rowspan="2">Precharge standby current in power-down mode</td><td>$I_{CC2}P$</td><td colspan="2">CKE ≤ V_{IL}(max), t_{CC} = 15ns</td><td colspan="5">2</td><td rowspan="2">mA</td><td rowspan="2"></td></tr>
<tr><td>$I_{CC2}PS$</td><td colspan="2">CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞</td><td colspan="5">2</td></tr>
<tr><td rowspan="2">Precharge standby current in non power-down mode</td><td>$I_{CC2}N$</td><td colspan="2">CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns
Input signals are changed one time during 30ns</td><td colspan="5">20</td><td>mA</td><td rowspan="2"></td></tr>
<tr><td>$I_{CC2}NS$</td><td colspan="2">CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞
Input signals are stable</td><td colspan="5">10</td><td>mA</td></tr>
<tr><td rowspan="2">Active standby current in power-down mode</td><td>$I_{CC3}P$</td><td colspan="2">CKE ≤ V_{IL}(max), t_{CC} = 15ns</td><td colspan="5">3</td><td rowspan="2">mA</td><td rowspan="2"></td></tr>
<tr><td>$I_{CC3}PS$</td><td colspan="2">CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞</td><td colspan="5">3</td></tr>
<tr><td rowspan="2">Active standby current in non power-down mode
(One bank active)</td><td>$I_{CC3}N$</td><td colspan="2">CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns
Input signals are changed one time during 30ns</td><td colspan="5">30</td><td>mA</td><td></td></tr>
<tr><td>$I_{CC3}NS$</td><td colspan="2">CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞
Input signals are stable</td><td colspan="5">20</td><td>mA</td><td></td></tr>
<tr><td rowspan="2">Operating current
(Burst mode)</td><td rowspan="2">I_{CC4}</td><td rowspan="2">I_o = 0 mA
Page burst
2 Banks activated</td><td>3</td><td>220</td><td>200</td><td>180</td><td>150</td><td>130</td><td rowspan="2">mA</td><td rowspan="2">2</td></tr>
<tr><td>2</td><td>-</td><td>-</td><td>-</td><td>130</td><td>110</td></tr>
<tr><td rowspan="2">Refresh current</td><td rowspan="2">I_{CC5}</td><td rowspan="2">t_{RC} ≥ t_{RC}(min)</td><td>3</td><td>200</td><td>200</td><td>180</td><td>160</td><td>150</td><td rowspan="2">mA</td><td rowspan="2">3</td></tr>
<tr><td>2</td><td>-</td><td>-</td><td>-</td><td>160</td><td>150</td></tr>
<tr><td rowspan="2">Self refresh current</td><td rowspan="2">I_{CC6}</td><td colspan="2" rowspan="2">CKE ≤ 0.2V</td><td colspan="5">2</td><td>mA</td><td>4</td></tr>
<tr><td colspan="5">450</td><td>uA</td><td>5</td></tr>
</table>

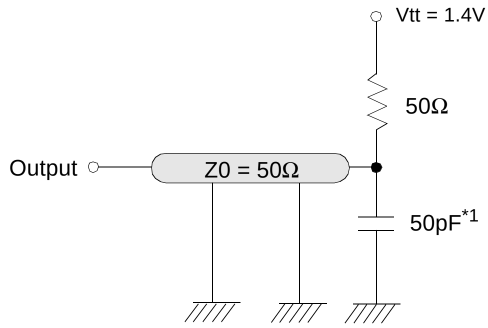
Notes : 1. Unless otherwise notes, Input level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}) in LVTTL.
2. Measured with outputs open.
3. Refresh period is 64ms.
4. K4S643232C-TC**
5. K4S643232C-TL**

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

Note : 1. The DC/AC Test Output Load of K4S643232C-55/60/70 is 30pF.
2. The VDD condition of K4S643232C-55/60 is 3.135V~3.6V.

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version										Unit	Note
		-55		-60		-70		-80		-10			
CAS Latency	CL	3	2	3	2	3	2	3	2	3	2	CLK	
CLK cycle time	tCC(min)	5.5	-	6	-	7	-	8	10	10	12	ns	
Row active to row active delay	tRRD(min)	2										CLK	1
$\overline{RAS}$ to $\overline{CAS}$ delay	tRCD(min)	3	-	3	-	3	-	3	2	2	2	CLK	1
Row precharge time	tRP(min)	3	-	3	-	3	-	3	2	2	2	CLK	1
Row active time	tRAS(min)	7	-	7	-	7	-	6	5	5	4	CLK	1
	tRAS(max)	100										us	
Row cycle time	tRC(min)	10	-	10	-	10	-	9	7	7	6	CLK	1
Row cycle time in Auto refresh	tRFC(min)	12	-	12	-	10	-	9	7	7	6	CLK	1,6
Last data in to row precharge	tRDL(min)	2										CLK	2, **5**
Last data in to new col.address delay	tCDL(min)	1										CLK	2
Last data in to burst stop	tBDL(min)	1										CLK	2
Col. address to col. address delay	tCCD(min)	1										CLK	
Mode Register Set cycle time	tMRS(min)	2										CLK	
Number of valid output data	CAS Latency=3	2										ea	4
	CAS Latency=2	1											

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer. Refer to the following ns-unit based AC table.

Parameter	Symbol	Version					Unit
		-55	-60	-70	-80	-10	
CLK cycle time	tCC(min)	5.5	6	7	8	10	ns
Row active to row active delay	tRRD(min)	11	12	14	16	20	ns
$\overline{RAS}$ to $\overline{CAS}$ delay	tRCD(min)	16.5	18	21	20	20	ns
Row precharge time	tRP(min)	16.5	18	21	20	20	ns
Row active time	tRAS(min)	38.5	42	49	48	48	ns
	tRAS(max)	100					us
Row cycle time	tRC(min)	55	60	70	70	70	ns
Row cycle time in Auto refresh	tRFC(min)	66	72	70	70	70	ns

2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -55/60/70/80/10, tRDL=1CLK product can be supported within restricted amounts and it will be distinguished by bucket code "NV". From the next generation, tRDL will be only 2CLK for every clock frequency.
6. A new command should be issued after self refersh exit followed by tRFC.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-55		-60		-70		-80		-10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS Latency=3	tCC	5.5	1000	6	1000	7	1000	8	1000	10	1000	ns	1
	CAS Latency=2		-		-		-		10		12			
CLK to valid output delay	CAS Latency=3	tSAC	-	5	-	5.5	-	5.5	-	6	-	6	ns	1, 2
	CAS Latency=2		-	-	-	-	-	-	-	6	-	8		
Output data		tOH	2	-	2.5	-	2.5	-	2.5	-	2.5	-	ns	2
CLK high pulse width	CAS Latency=3	tCH	2	-	2.5	-	3	-	3	-	3.5	-	ns	3
	CAS Latency=2		-	-	-									
CLK low pulse width	CAS Latency=3	tCL	2	-	2.5	-	3	-	3	-	3.5	-	ns	3
	CAS Latency=2		-	-	-									
Input setup time	CAS Latency=3	tSS	1.5	-	1.5	-	1.75	-	2	-	2.5	-	ns	3
	CAS Latency=2		-	-	-		-							
Input hold time		tSH	1	-	1	-	1	-	1	-	1	-	ns	3
CLK to output in Low-Z		tSLZ	1	-	1	-	1	-	1	-	1	-	ns	2
CLK to output in Hi-Z	CAS Latency=3	tSHZ	-	5	-	5.5	-	5.5	-	6	-	6	ns	
	CAS Latency=2		-	-	-	-	-	-	-	6	-	8		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	$A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don′t care, H=Logic high, L=Logic low)

Notes :1. OP Code : Operand code
$A_0 \sim A_{10}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	BA_0 ~ BA_1	A_{10}/AP	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Function	RFU	RFU	W.B.L	TM		CAS Latency			BT	Burst Length		

Test Mode		
A_8	A_7	Type
0	0	Mode Register Set
0	1	Reserved
1	0	Reserved
1	1	Reserved

Write Burst Length	
A_9	Length
0	Burst
1	Single Bit

CAS Latency			
A_6	A_5	A_4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Type	
A_3	Type
0	Sequential
1	Interleave

Burst Length				
A_2	A_1	A_0	BT = 0	BT = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

Full Page Length : x32 (256)

POWER UP SEQUENCE

SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Apply power and start clock. Must maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

Note : 1. If A_9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
2. RFU (Reserved for future use) should stay "0" during MRS cycle.

BURST SEQUENCE (BURST LENGTH = 4)

Initial Address		Sequential				Interleave			
A_1	A_0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

BURST SEQUENCE (BURST LENGTH = 8)

Initial Address			Sequential								Interleave							
A_2	A_1	A_0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

DEVICE OPERATIONS

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high all inputs are assumed to be in a valid state (low or high) for the duration of set-up and hold time around positive edge of the clock in order to function well Q perform and I_{CC} specifications.

CLOCK ENABLE (CKE)

The clock enable(CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time are the-same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1CLK + t_{SS}" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

BANK ADDRESSES (BA0 ~ BA1)

This SDRAM is organized as four independent banks of 524,288 words x 32 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0 ~ A10)

The 19 address bits are required to decode the 524,288 word locations are multiplexed into 11 address input pins (A_0 ~ A_{10}). The 11 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 8 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, the SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

POWER-UP

SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Apply power and start clock. Must maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for both banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

DEVICE OPERATIONS (Continued)

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A_0 ~ A_{10} and BA_0 ~ BA_1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on the fields of functions. The burst length field uses A_0 ~ A_2, burst type uses A_3, CAS latency (read latency from column address) use A_4 ~ A_6, vendor specific options or test mode use A_7 ~ A_8, A_{10}/AP and BA_0 ~ BA_1. The write burst length is programmed using A_9. A_7 ~ A_8, A_{10}/AP and BA_0 ~ BA_1 must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and CAS latencies.

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of t_{RCD}(min) from the time of bank activation. t_{RCD} is an internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing t_{RCD}(min) with cycle time of the clock and then rounding off the result to the next higher integer. The SDRAM has four internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of four banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high, requiring some time for power supplies to recover before another bank can be sensed reliably. t_{RRD}(min) specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t_{RAS}(min). Every SDRAM bank activate command must satisfy t_{RAS}(min) specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t_{RAS}(max). The number of cycles for both t_{RAS}(min) and t_{RAS}(max) can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{CAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least t_{RCD}(min) before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of the burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

BURST WRITE

The burst write command is similar to burst read command and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing can be completed yet. The writing can be completed by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and procreating the bank t_{RDL} after the last data input to be written into the active row. See DQM OPERATION also.

DEVICE OPERATIONS (Continued)

DQM OPERATION

The DQM is used to mask input and output operations. It works similar to $\overline{OE}$ during read operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interruptions of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is not required. Please refer to DQM timing diagram also.

PRECHARGE

The precharge operation is performed on an active bank by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A_{10}/AP with valid BA_0 ~ BA_1 of the bank to be precharged. The precharge command can be asserted anytime after t_{RAS}(min) is satisfied from the bank active command in the desired bank. t_{RP} is defined as the minimum number of clock cycles required to complete row precharge is calculated by dividing t_{RP} with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by t_{RAS}(max). Therefore, each bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to Power down, Auto refresh, Self refresh and Mode register set etc. is possible only when all banks are in idle state.

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy t_{RAS}(min) and "t_{RP}" for the programmed burst length and $\overline{CAS}$ latency. The auto precharge command is issued at the same time as burst read or burst write by asserting high on A_{10}/AP. If burst read or burst write by asserting high on A_{10}/AP, the bank is left active until a new command is asserted. Once auto precahrge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

BOTH BANKS PRECHARGE

Both banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ with high on A_{10}/AP after all banks have satisfied t_{RAS}(min) requirement, performs precharge on all banks. At the end of t_{RP} after performing precharge to all the banks, both banks are in idle state.

AUTO REFRESH

The storage cells of SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by t_{RFC}(min). The minimum number of clock cycles required can be calculated by driving t_{RFC} with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. All banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6us or a burst of 4096 auto refresh cycles once in 64ms.

SELF REFRESH

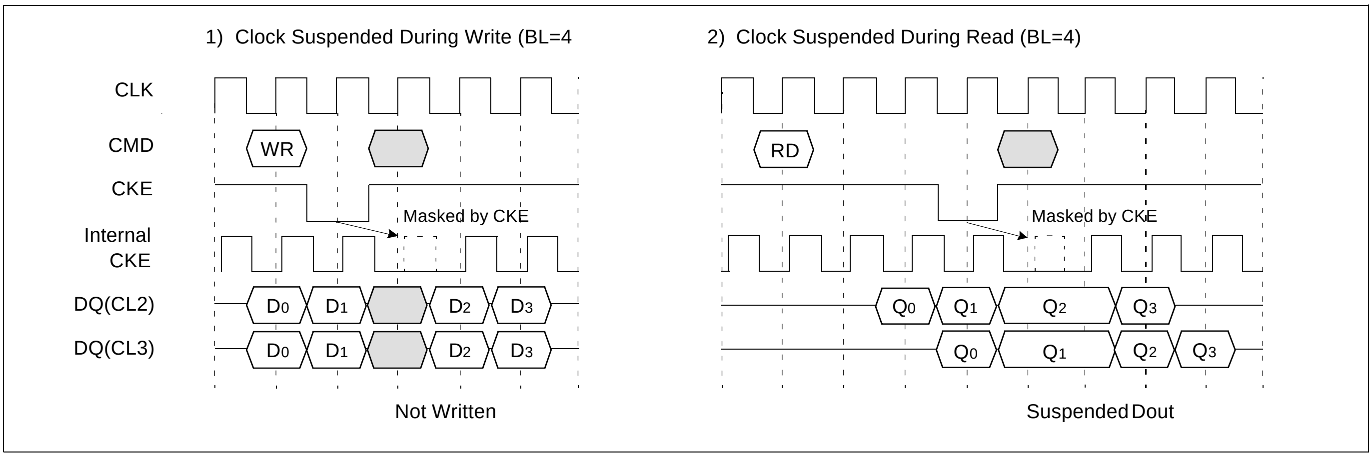
The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing are internally generated to reduce power consumption.

The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including the clock are ignored in order to remain in the self refresh mode.

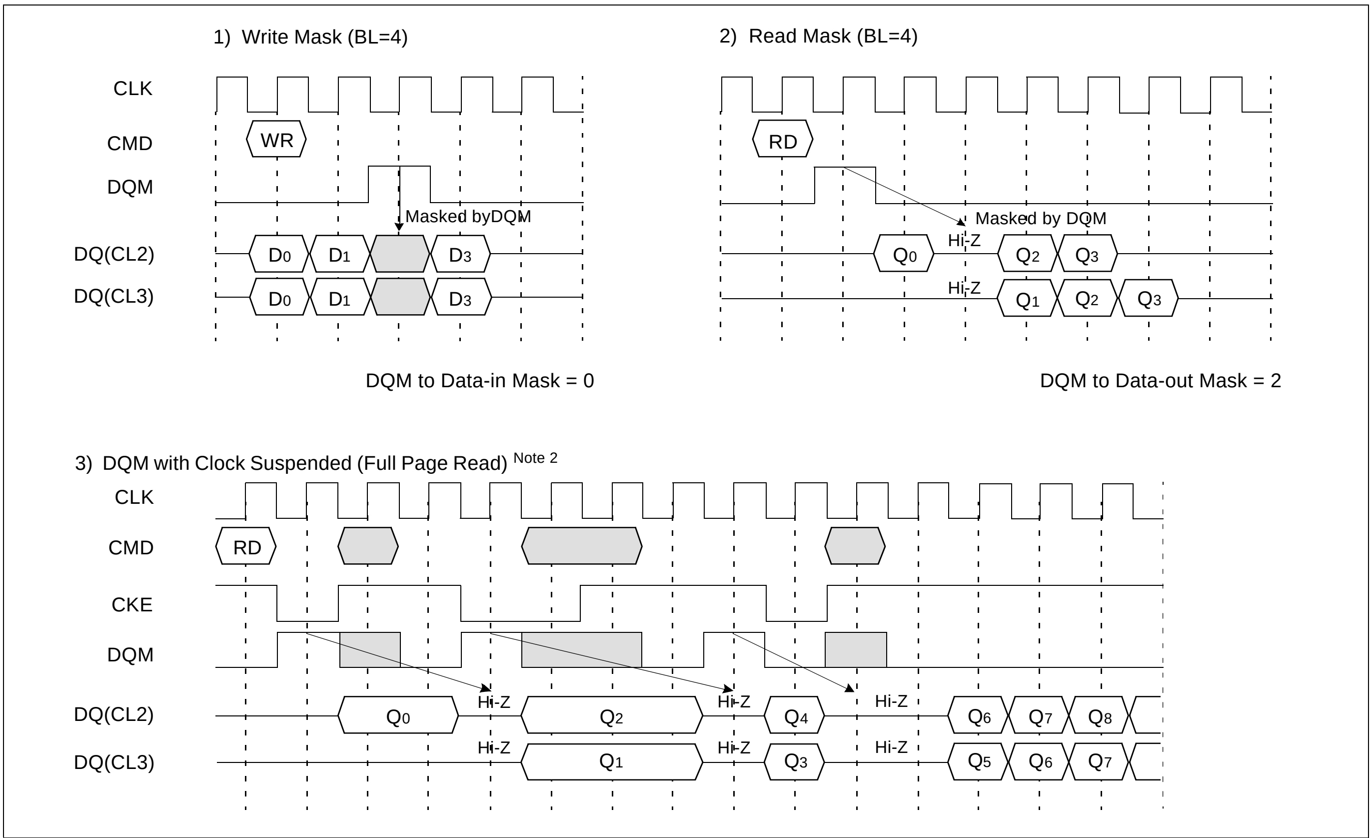
The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of t_{RFC} before the SDRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 4096 auto refresh cycles immediately after exiting in self refresh mode.

BASIC FEATURE AND FUNCTION DESCRIPTIONS

1. CLOCK Suspend

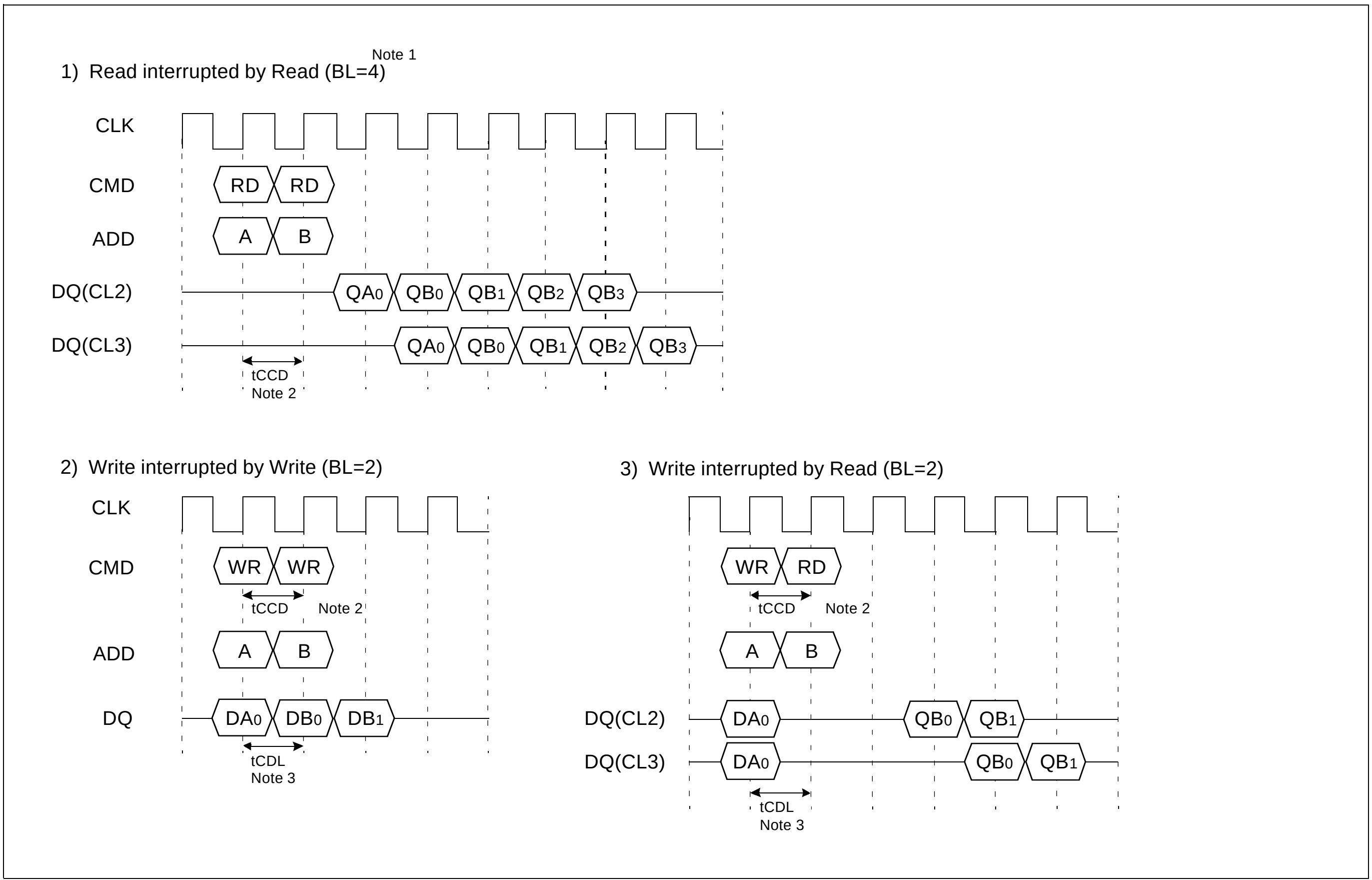


2. DQM Operation



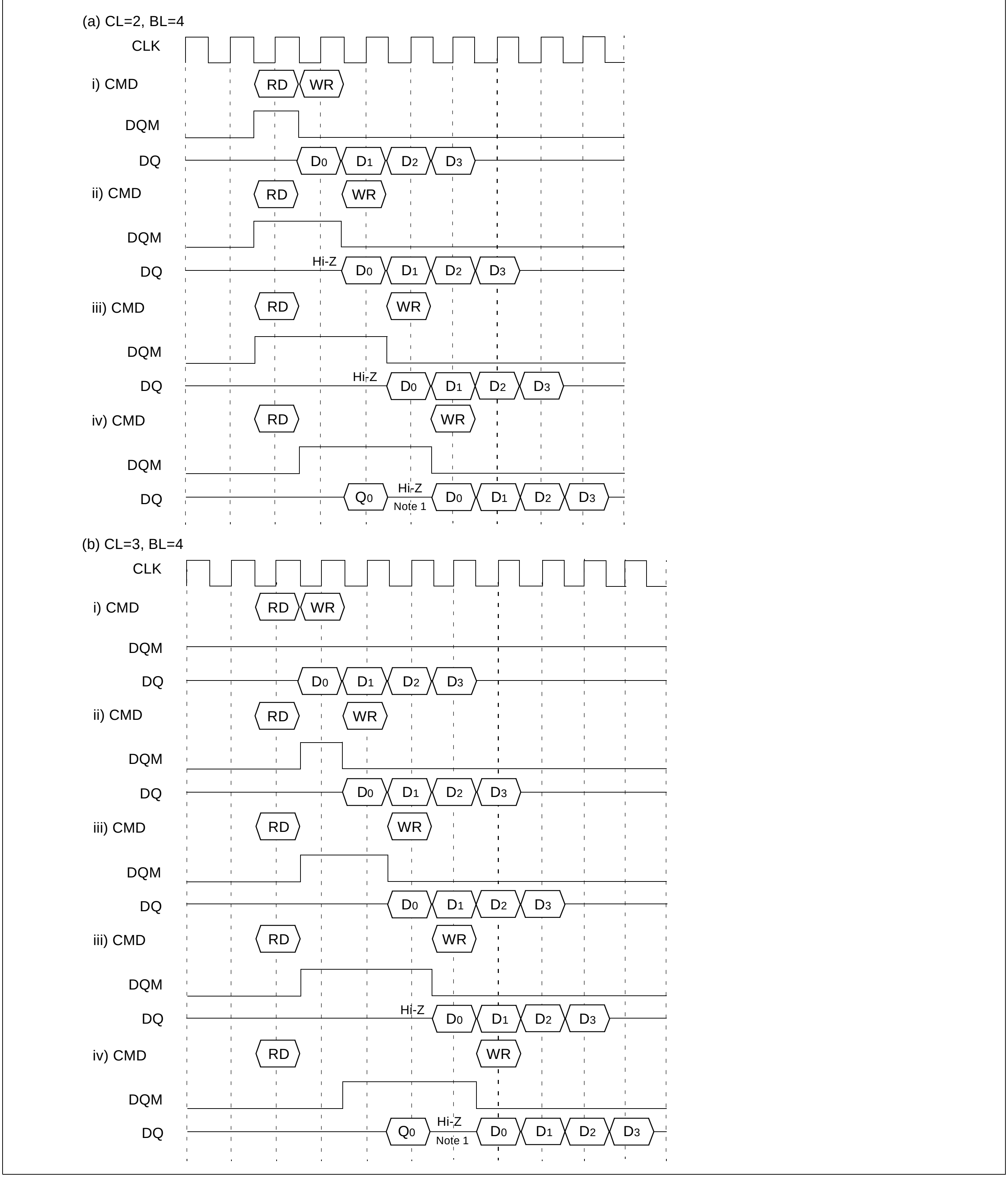
***Note :** 1. CKE to CLK disable/enable = 1CLK.
2. DQM makes data out Hi-Z after 2CLKs which should masked by CKE " L"
3. DQM masks both data-in and data-out.

3. $\overline{CAS}$ Interrupt (I)



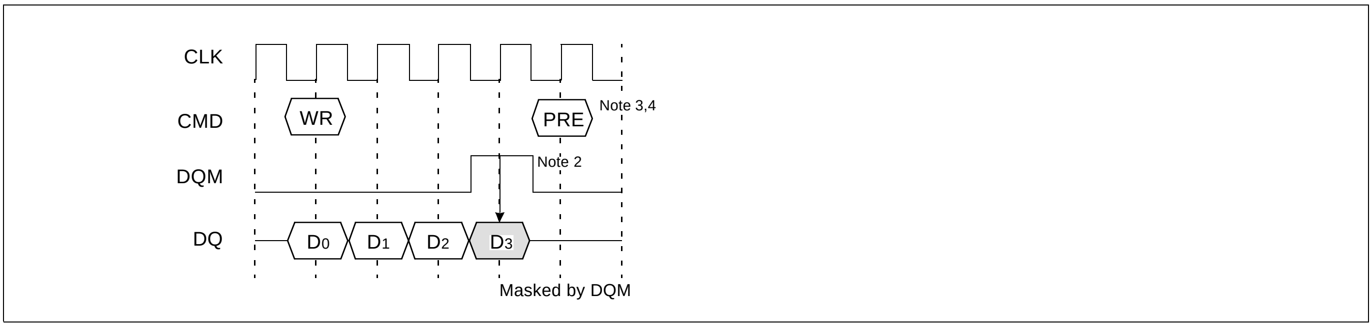
***Note :** 1. By " Interrupt", It is meant to stop burst read/write by external command before the end of burst.
By "$\overline{CAS}$ Interrupt", to stop burst read/write by $\overline{CAS}$ access ; read and write.
2. t_{CCD} : $\overline{CAS}$ to $\overline{CAS}$ delay. (=1CLK)
3. t_{CDL} : Last data in to new column address delay. (=1CLK)

4. CAS Interrupt (II) : Read Interrupted by Write & DQM



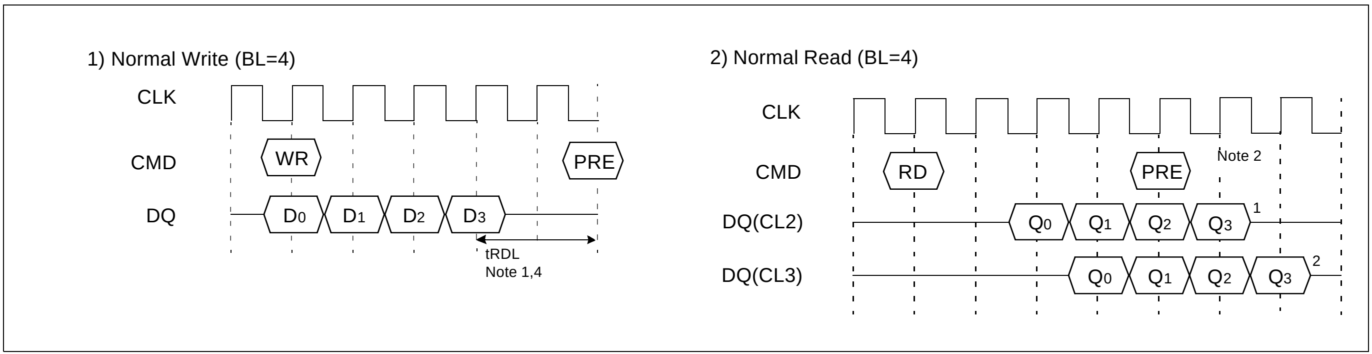
***Note :** 1. To prevent bus contention, there should be at least one gap between data in and data out.

5. Write Interrupted by Precharge & DQM

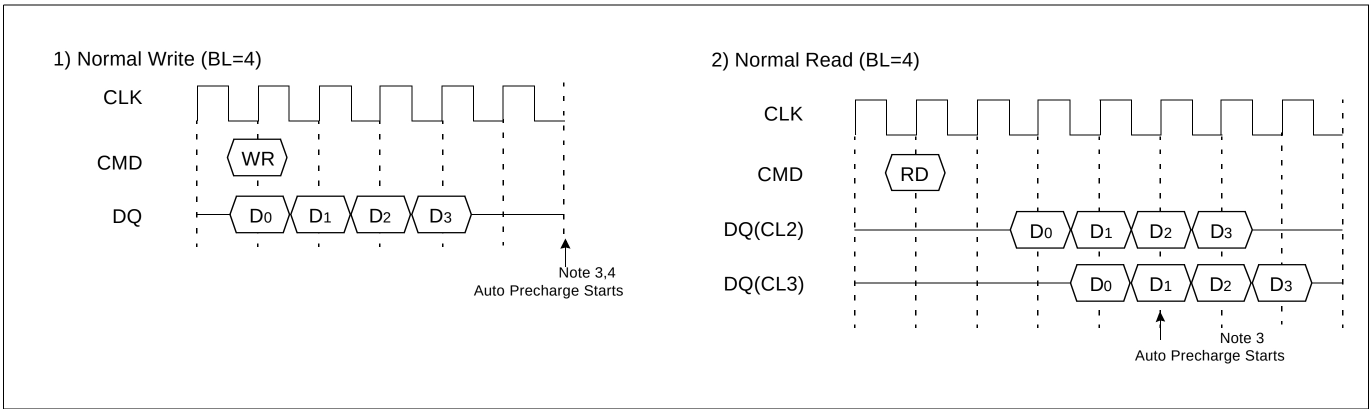


*Note : 1. To prevent bus contention, DQM should be issued which makes at least one gap between data in and data out.
2. To inhibit invalid write, DQM should be issued.
3. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of four banks operation.
4. For -55/60/70/80/10, tRDL=1CLK product can be supported within restricted amounts and it will be distinguished by bucket code "NV"
. From the next generation, tRDL will be only 2CLK for every clock frequency.

6. Precharge

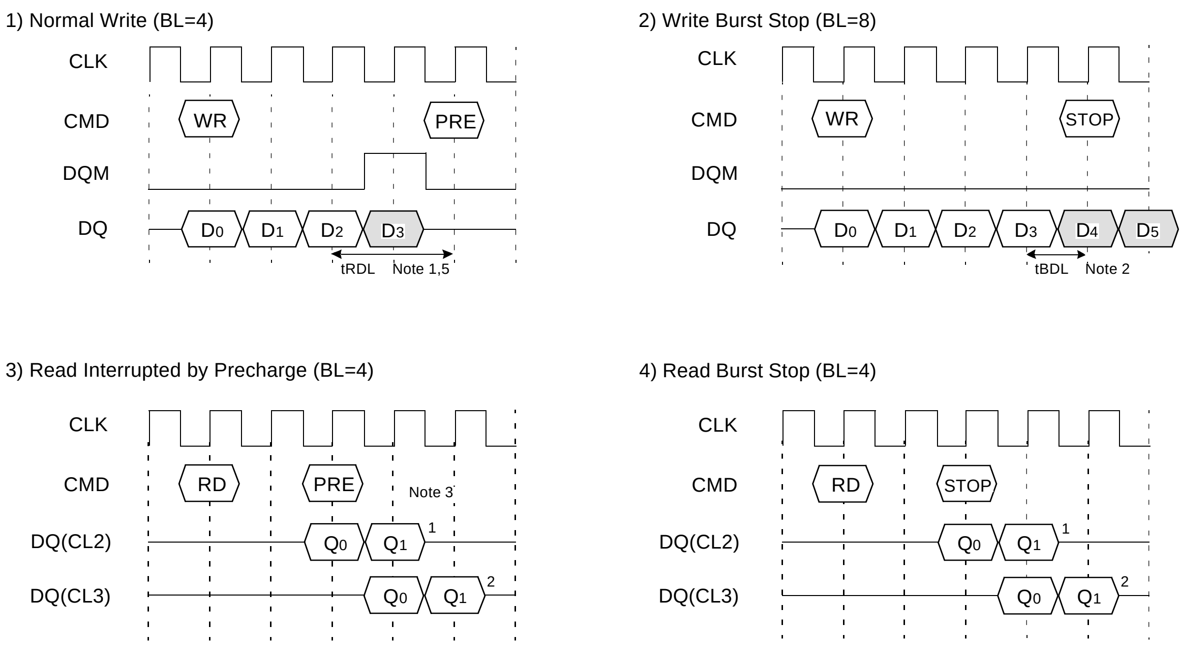


7. Auto Precharge

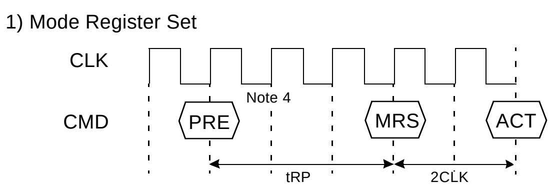


*Note : 1. tRDL : Last data in to row precharge delay
2. Number of valid output data after row precharge : 1, 2 for CAS Latency = 2, 3 respectively.
3. The row active command of the precharge bank can be issued after tRP from this point.
The new read/write command of other activated bank can be issued from this point.
At burst read/write with auto precharge, CAS interrupt of the same/another bank is illegal.
4. For -55/60/70/80/10, tRDL=1CLK product can be supported within restricted amounts and it will be distinguished by bucket code "NV"
. From the next generation, tRDL will be only 2CLK for every clock frequency

8. Burst Stop & Interrupted by Precharge



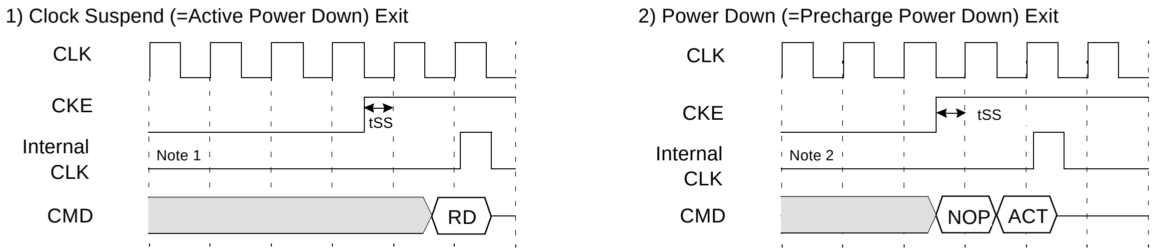
9. MRS



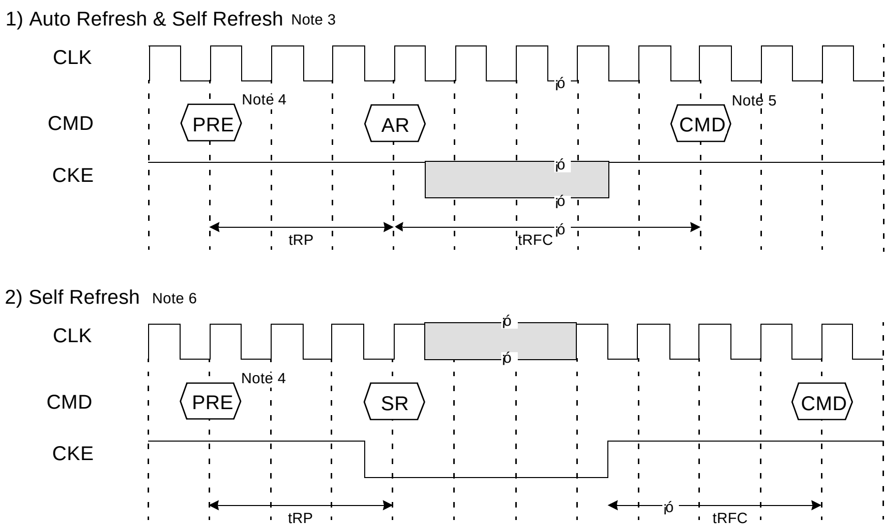
***Note :** 1. tRDL : 1 CLK

2. tBDL : 1 CLK ; Last data in to burst stop delay.
   Read or write burst stop command is valid at every burst length.
3. Number of valid output data after row precharge or burst stop : 1, 2 for CAS latency= 2, 3 respectiviely.
4. PRE : All banks precharge if necessary.
   MRS can be issued only at all banks precharge state.
5. For -55/60/70/80/10, tRDL=1CLK product can be supported within restricted amounts and it will be distinguished by bucket code "NV"
   . From the next generation, tRDL will be only 2CLK for every clock frequency

10. Clock Suspend Exit & Power Down Exit



11. Auto Refresh & Self Refresh



***Note :** 1. Active power down : one or more banks active state.
2. Precharge power down : all banks precharge state.
3. The auto refresh is the same as CBR refresh of conventional DRAM.
No precharge commands are required after auto refresh command.
During t_{RFC} from auto refresh command, any other command can not be accepted.
4. Before executing auto/self refresh command, all banks must be idle state.
5. MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
6. During self refresh mode, refresh interval and refresh operation are perfomed internally.
After self refresh entry, self refresh mode is kept while CKE is low.
During self refresh mode, all inputs expect CKE will be don't cared, and outputs will be in Hi-Z state.
For the time interval of t_{RFC} from self refresh exit command, any other command can not be accepted.
Before/After self refresh mode, burst auto refresh cycle (4096 cycles) is recommended.

12. About Burst Type Control

Basic MODE	Sequential Counting	At MRS A_3 = "0". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=1, 2, 4, 8 and full page.
	Interleave Counting	At MRS A_3 = "1". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=4, 8. At BL=1, 2 Interleave Counting = Sequential Counting
Random MODE	Random column Access t_{CCD} = 1 CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of conventional DRAM.

13. About Burst Length Control

Basic MODE	1	At MRS $A_{2,1,0}$ = "000". At auto precharge, t_{RAS} should not be violated.
	2	At MRS $A_{2,1,0}$ = "001". At auto precharge, t_{RAS} should not be violated.
	4	At MRS $A_{2,1,0}$ = "010".
	8	At MRS $A_{2,1,0}$ = "011".
	Full Page	At MRS $A_{2,1,0}$ = "111". Wrap around mode(Infinite burst length) should be stopped by burst stop $\overline{RAS}$ interrupt or $\overline{CAS}$ interrupt
Special MODE	BRSW	At MRS A_9 = "1". Read burst =1, 2, 4, 8, full page write Burst =1 At auto precharge of write, t_{RAS} should not be violated.
Random MODE	Burst Stop	t_{BDL}= 1, Valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively Using burst stop command, any burst length control is possible.
Interrupt MODE	$\overline{RAS}$ Interrupt (Interrupted by Precharge)	Before the end of burst, Row precharge command of the same bank stops read/write burst with Row precharge. t_{RDL}= 2 with DQM, valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively. During read/write burst with auto precharge, $\overline{RAS}$ interrupt can not be issued.
	$\overline{CAS}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst. During read/write burst with auto precharge, $\overline{CAS}$ interrupt can not be issued.

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	**Note**
IDLE	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA, A_{10}/AP	ILLEGAL	2
	L	L	H	H	BA	RA	Row (& Bank) Active ; Latch RA	
	L	L	H	L	BA	A_{10}/AP	NOP	4
	L	L	L	H	X	X	Auto Refresh or Self Refresh	5
	L	L	L	L	OP code	OP code	Mode Register Access	5
Row Active	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	BA	CA, A_{10}/AP	Begin Read ; latch CA ; determine AP	
	L	H	L	L	BA	CA, A_{10}/AP	Begin Write ; latch CA ; determine AP	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	Precharge	
	L	L	L	X	X	X	ILLEGAL	
Read	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A_{10}/AP	Term burst, New Read, Determine AP	
	L	H	L	L	BA	CA, A_{10}/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	Term burst, Precharge timing for Reads	
	L	L	L	X	X	X	ILLEGAL	
Write	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A_{10}/AP	Term burst, New read, Determine AP	3
	L	H	L	L	BA	CA, A_{10}/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	Term burst, precharge timing for Writes	3
	L	L	L	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A_{10}/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA_{10}	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A_{10}/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA_{10}	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Pre-charging	H	X	X	X	X	X	NOP --> Idle after t_{RP}	
	L	H	H	H	X	X	NOP --> Idle after t_{RP}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	NOP --> Idle after t_{RP}L	4

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	Note
Row Activating	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	H	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Refreshing	H	X	X	X	X	X	NOP --> Idle after t_{RFC}	
	L	H	H	X	X	X	NOP --> Idle after t_{RFC}	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	NOP --> Idle after 2 clocks	
	L	H	H	H	X	X	NOP --> Idle after 2 clocks	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

Abbreviations : RA = Row Address BA = Bank Address
NOP = No Operation Command CA = Column Address AP = Auto Precharge

***Note :** 1. All entries assume the CKE was active (High) during the precharge clcok and the current clock cycle.
2. Illegal to bank in specified state ; Function may be Iegal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA (and A_{10}/AP).
5. Illegal if any bank is not idle.

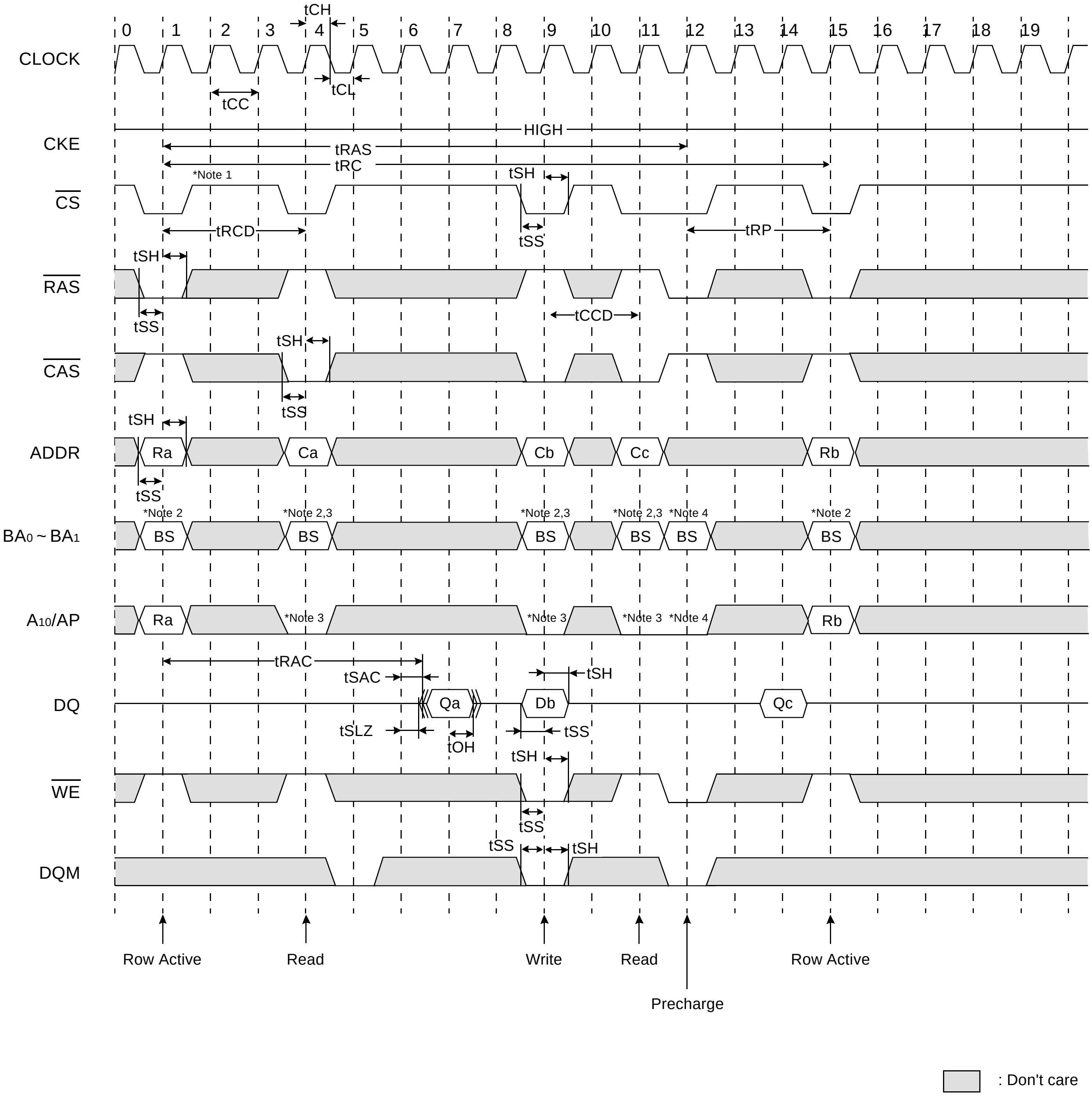
FUNCTION TRUTH TABLE (TABLE 2)

Current State	CKE (n-1)	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	ACTION	Note
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh --> Idle after t_{RFC} (ABI)	6
	L	H	L	H	H	H	X	Exit Self Refresh --> Idle after t_{RFC} (ABI)	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	
All Banks Precharge Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Power Down --> ABI	
	L	H	L	H	H	H	X	Exit Power Down --> ABI	7
	L	H	L	H	H	L	X	ILLEGAL	7
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Low Power Mode)	
All Banks Idle	H	H	X	X	X	X	X	Refer to Table 1	
	H	L	H	X	X	X	X	Enter Power Down	
	H	L	L	H	H	H	X	Enter Power Down	8
	H	L	L	H	H	L	X	ILLEGAL	8
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row (& Bank) Active	
	H	L	L	L	L	H	X	Enter Self Refresh	8
	H	L	L	L	L	L	OP Code	Mode Register Access	
	L	L	X	X	X	X	X	NOP	
Any State other than Listed above	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain Clcok Suspend	

Abbreviations : ABI = All Banks Idle, RA = Row Address

***Note :** 6. CKE low to high transition is asynchronous.
7. CKE low to high transition is asynchronous if restarts internal clock.
A minimum setup time 1CLK + t_{SS} must be satisfied before any command other than exit.
8. Power down and self refresh can be entered only from the both banks idle state.
9. Must be a legal command.

Single Bit Read-Write-Read Cycle(Same Page) @CAS Latency=3, Burst Length=1



***Note :** 1. All input expect CKE & DQM can be don't care when $\overline{CS}$ is high at the CLK high going edge.
2. Bank active & read/write are controlled by BA0~BA1.

BA0	BA1	Active & Read/Write
0	0	Bank A
0	1	Bank B
1	0	Bank C
1	1	Bank D

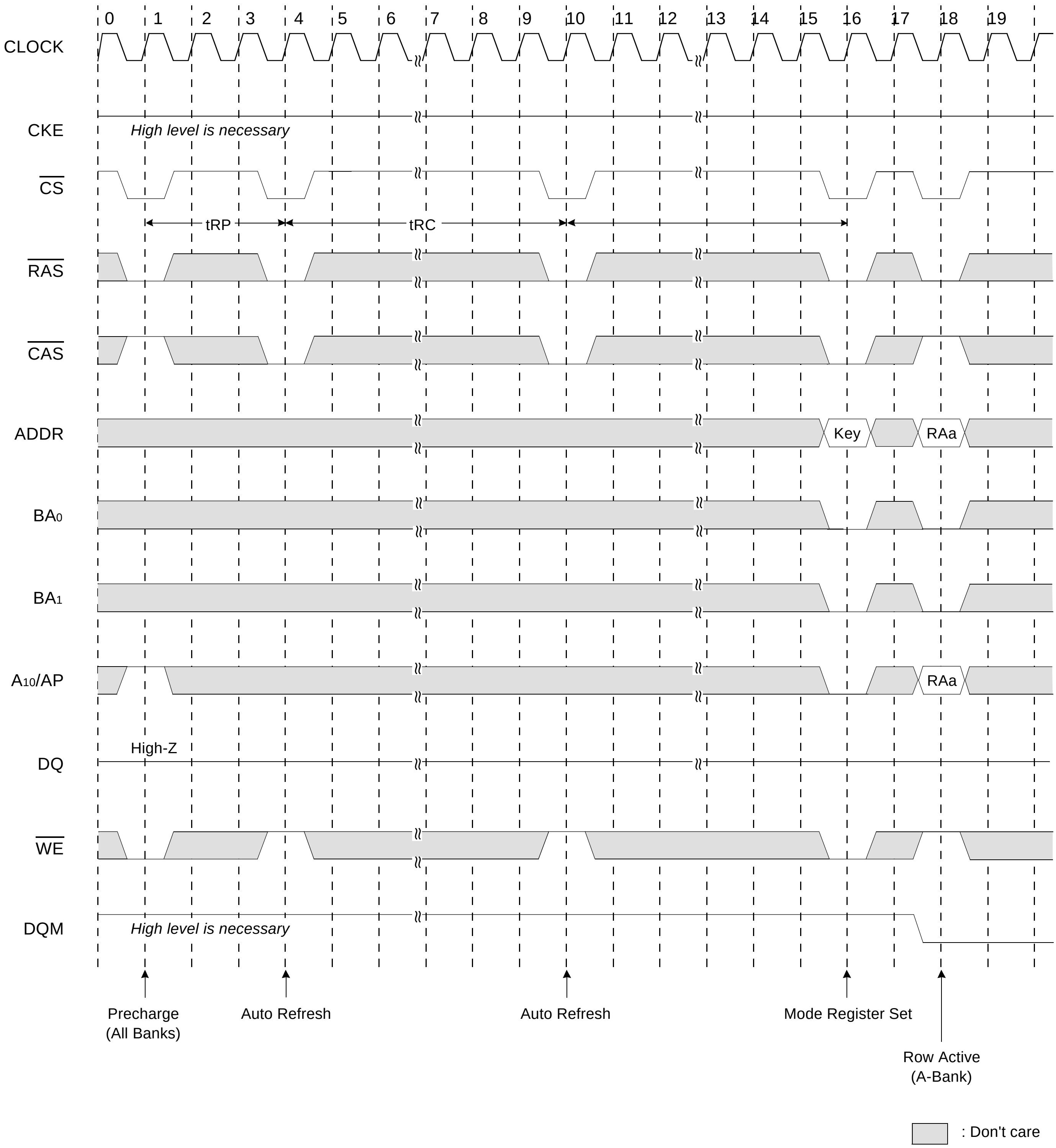
3. Enable and disable auto precharge function are controlled by A10/AP in read/write command

A10/AP	BA0	BA1	Operation
0	0	0	Disable auto precharge, leave bank A active at end of burst.
	0	1	Disable auto precharge, leave bank B active at end of burst.
	1	0	Disable auto precharge, leave bank C active at end of burst.
	1	1	Disable auto precharge, leave bank D active at end of burst.
1	0	0	Enable auto precharge, precharge bank A at end of burst.
	0	1	Enable auto precharge, precharge bank B at end of burst.
	1	0	Enable auto precharge, precharge bank C at end of burst.
	1	1	Enable auto precharge, precharge bank D at end of burst.

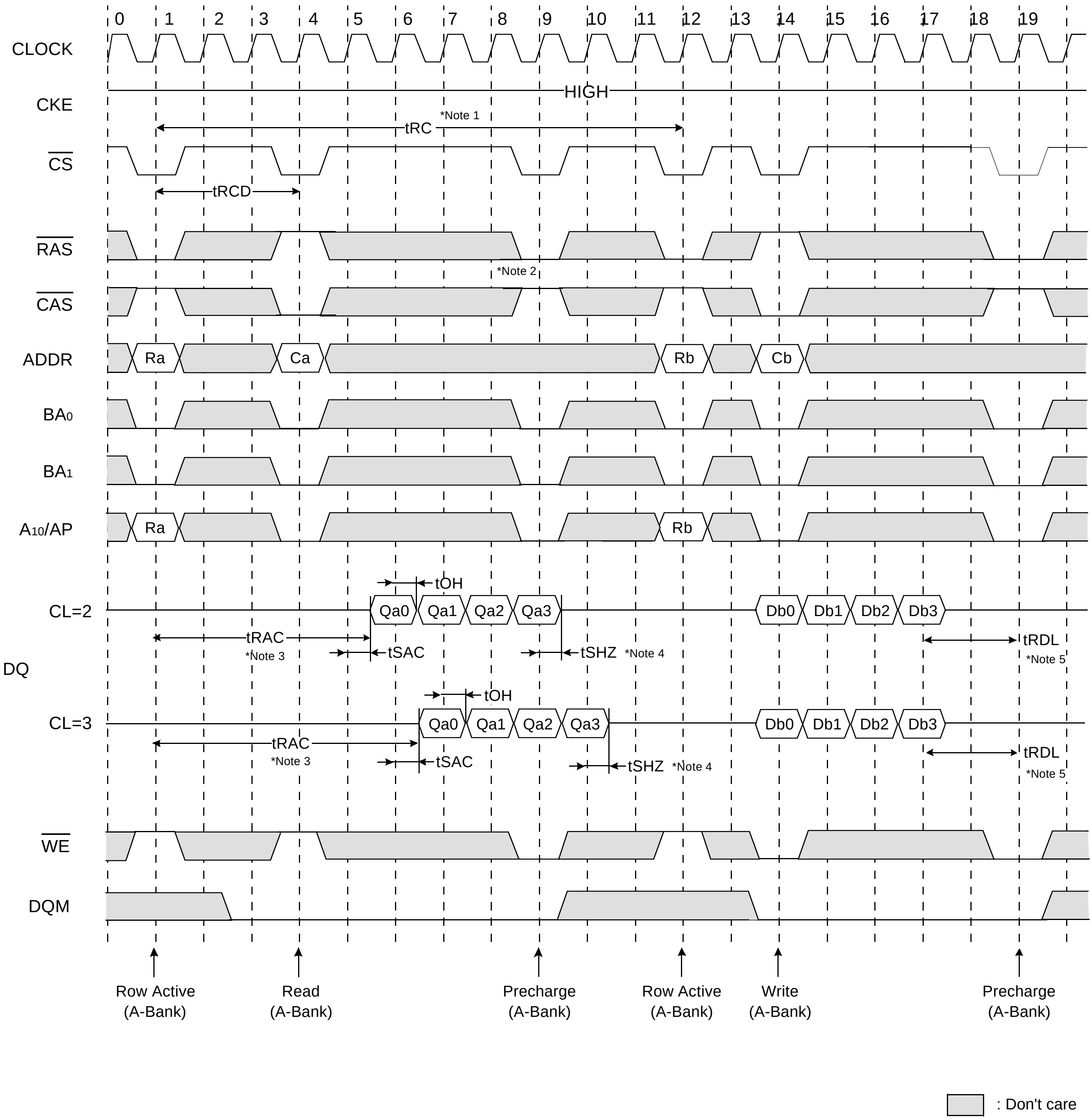
4. A10/AP and BA0~BA1 control bank precharge when precharge command is asserted.

A10/AP	BA0	BA1	Precharge
0	0	0	Bank A
0	0	0	Bank B
0	1	1	Bank C
0	1	1	Bank D
1	x	x	All Banks

Power Up Sequence

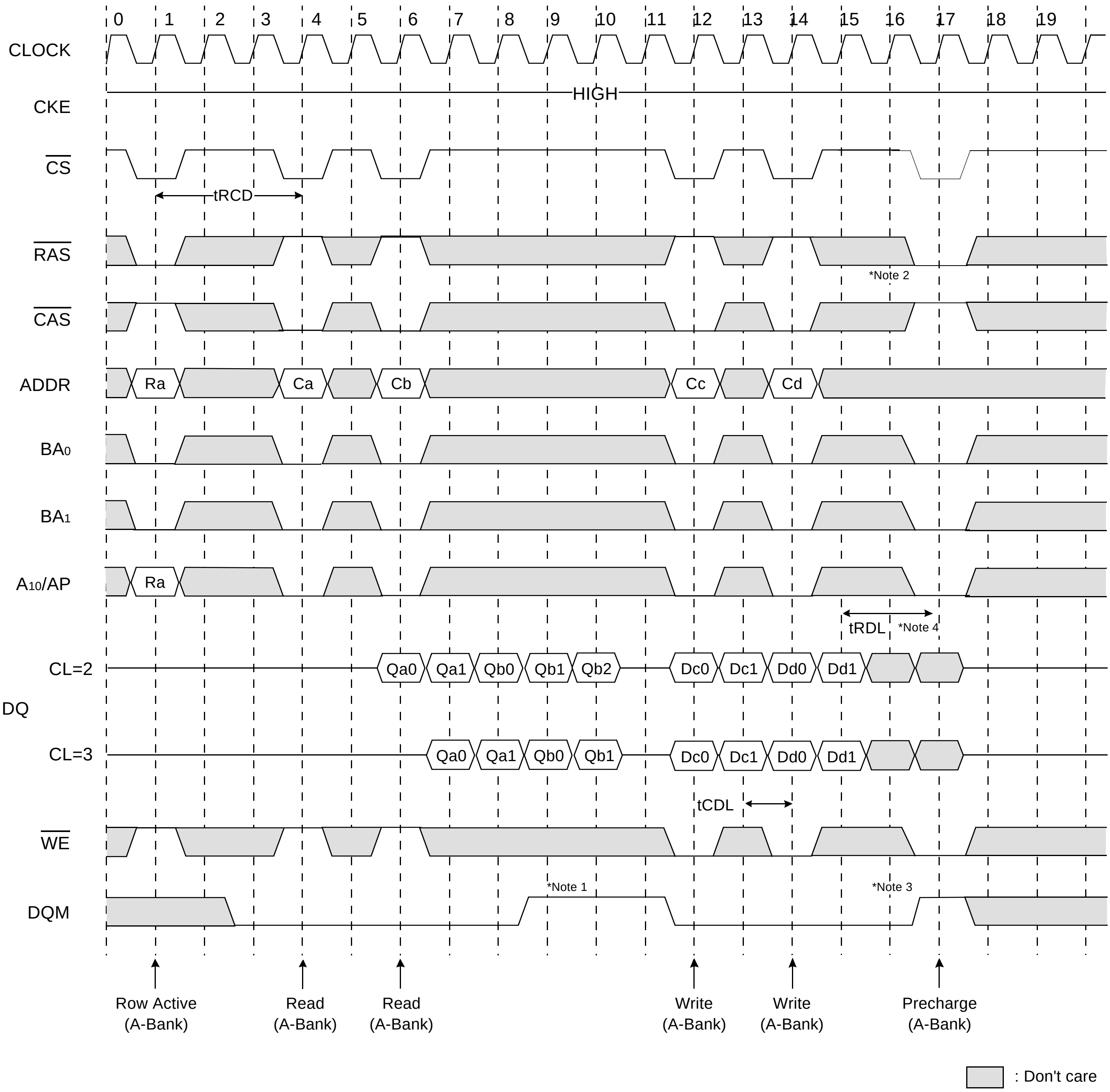


Read & Write Cycle at Same Bank @Burst Length=4



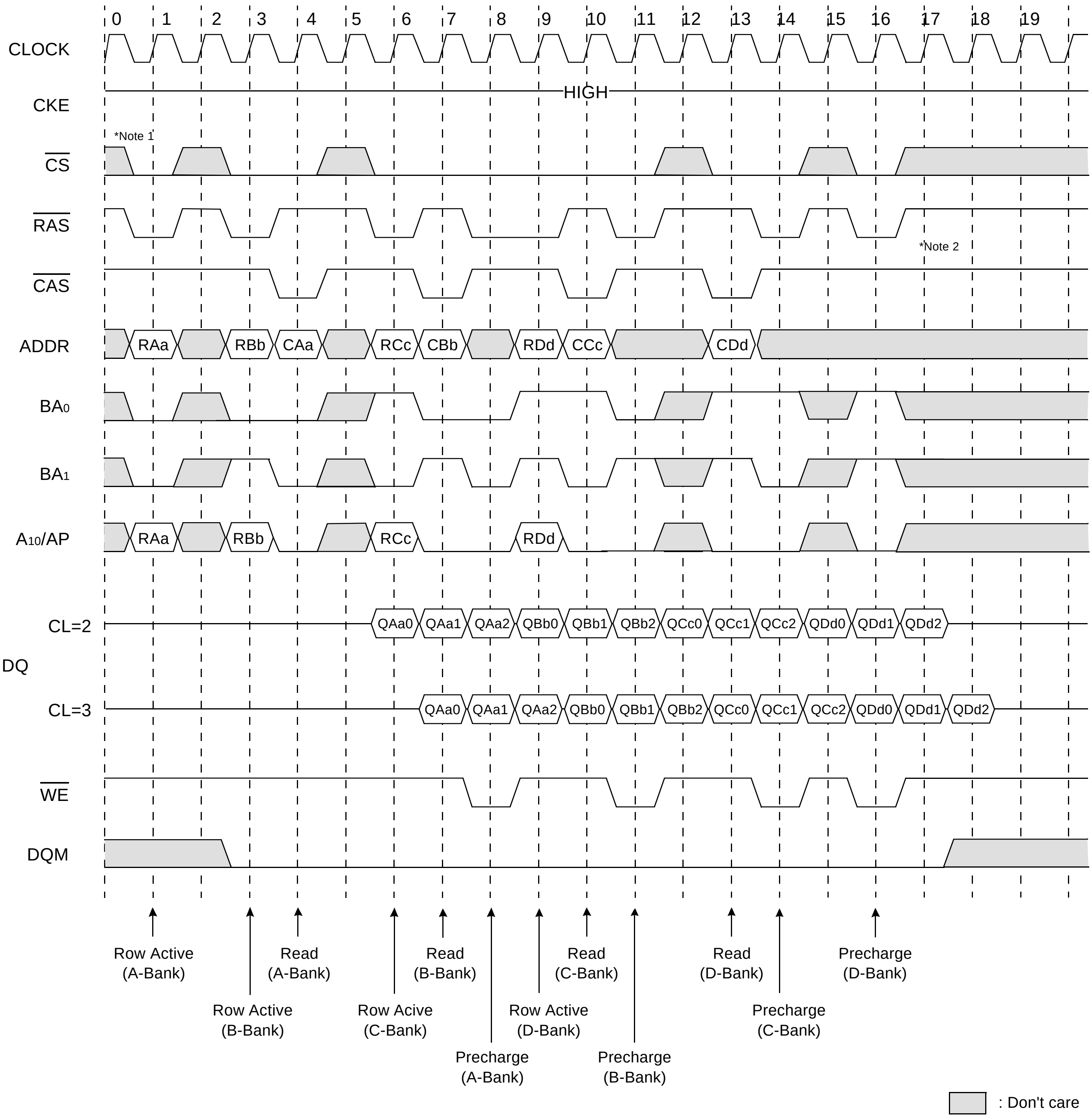
***Note :**
1. Minimum row cycle times is required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clcok.
3. Access time from Row active command. t_{CC} *(t_{RCD} + CAS latency - 1) + t_{SAC}
4. Ouput will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)
5. For -55/60/70/80/10, tRDL=1CLK product can be supported within restricted amounts and it will be distinguished by bucket code "NV". From the next generation, tRDL will be only 2CLK for every clock frequency

Page Read & Write Cycle at Same Bank @Burst Length=4



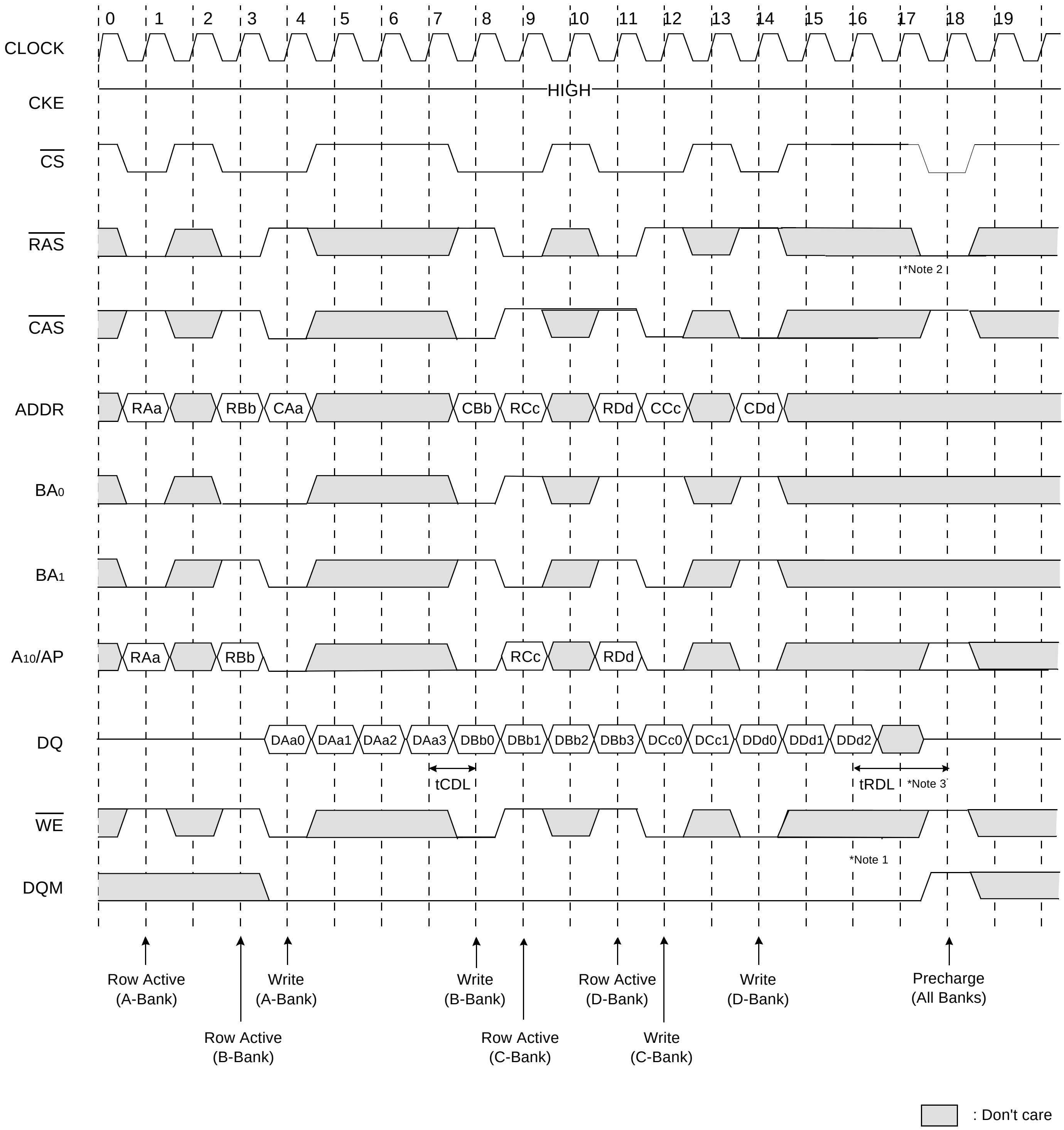
***Note :**
1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, tRDL before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
4. For -55/60/70/80/10, tRDL=1CLK product can be supported within restricted amounts and it will be distinguished by bucket code "NV". From the next generation, tRDL will be only 2CLK for every clock frequency

Page Read Cycle at Different Bank @Burst Length=4



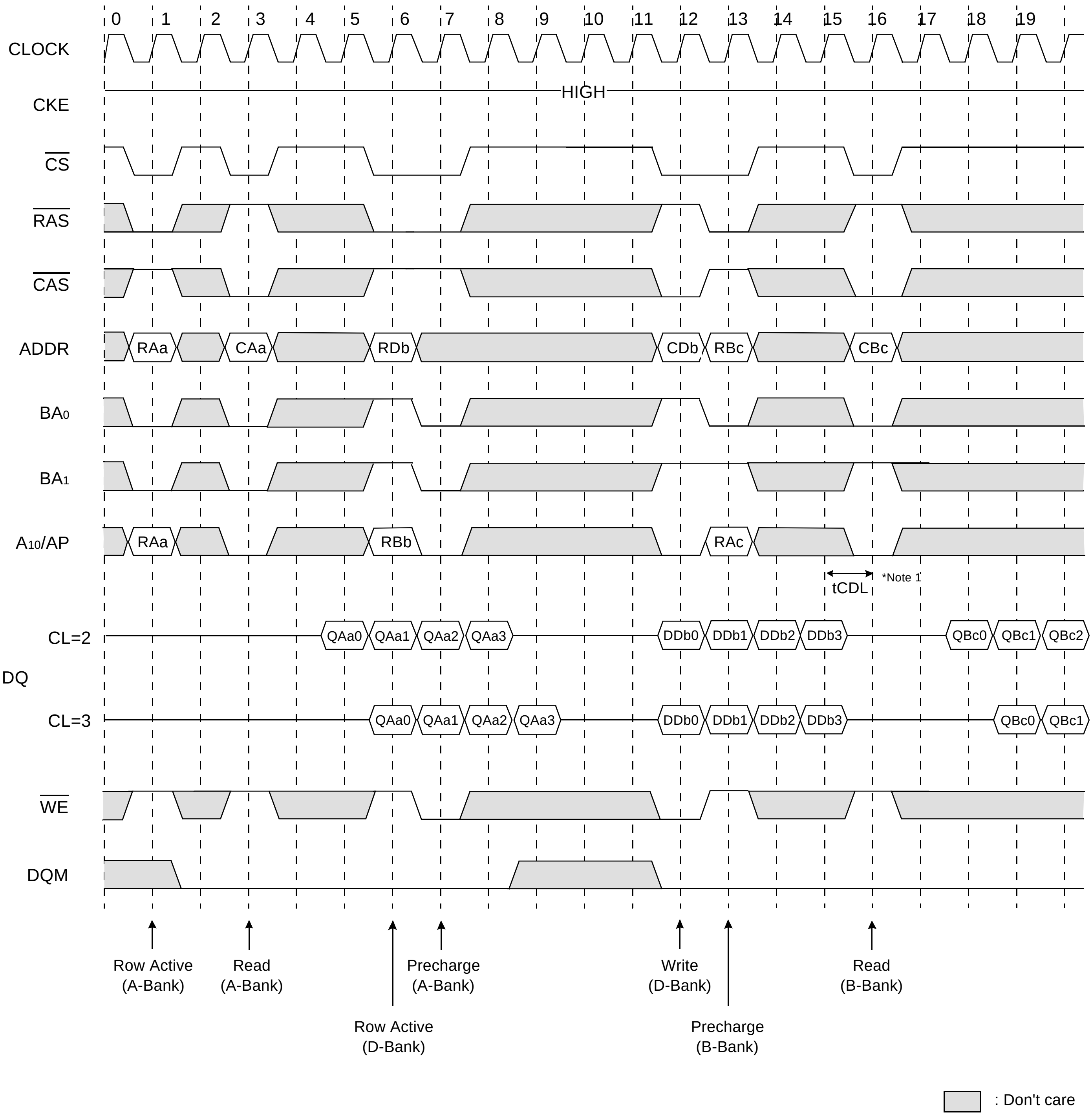
***Note :** 1. CS can be don't cared when RAS, CAS and WE are high at the clock high going dege.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

Page Write Cycle at Different Bank @Burst Length=4



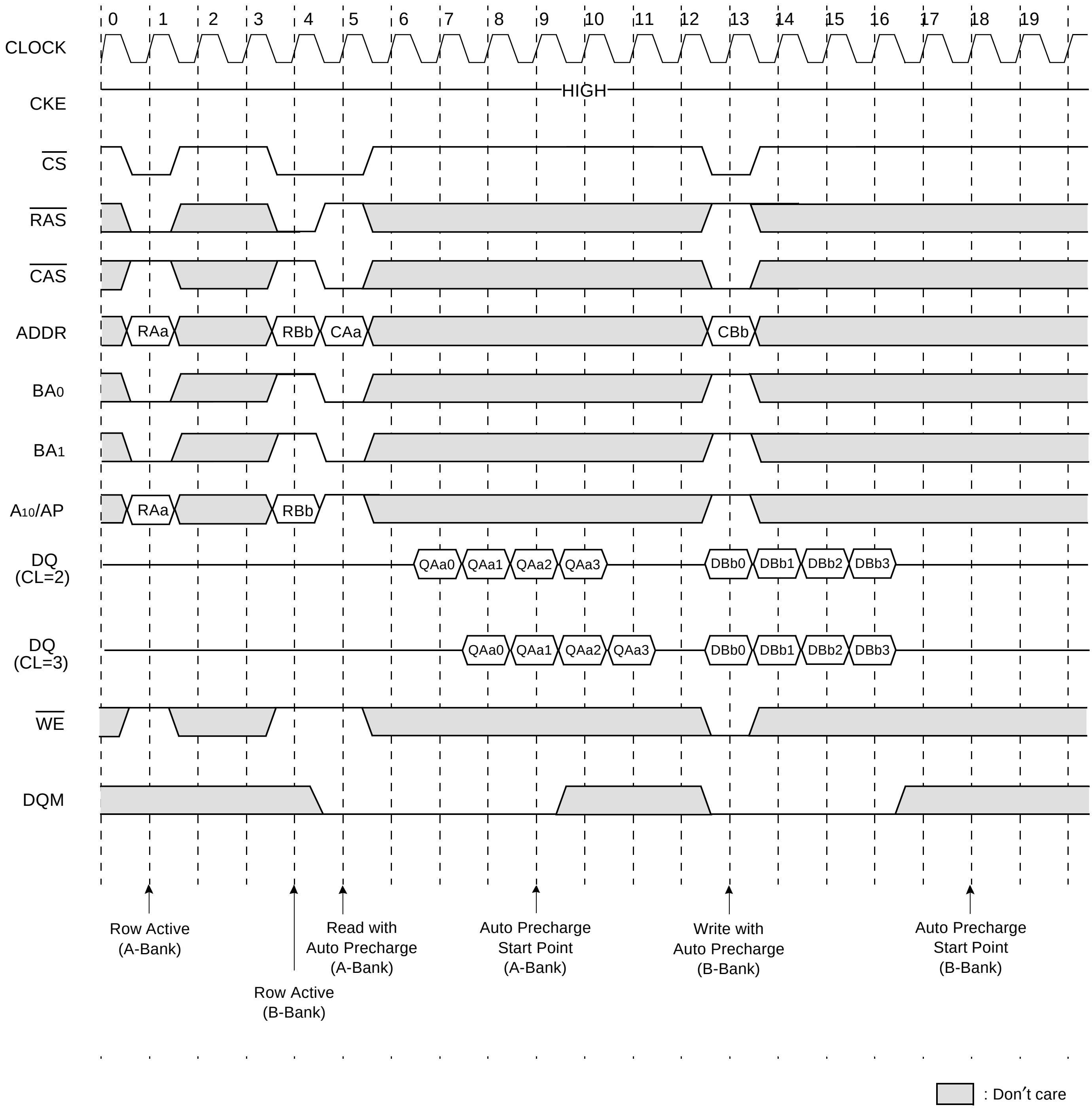
***Note :** 1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.
3.For -55/60/70/80/10, tRDL=1CLK product can be supported within restricted amounts and it will be distinguished by bucket code "NV". From the next generation, tRDL will be only 2CLK for every clock frequency

Read & Write Cycle at Different Bank @Burst Length=4



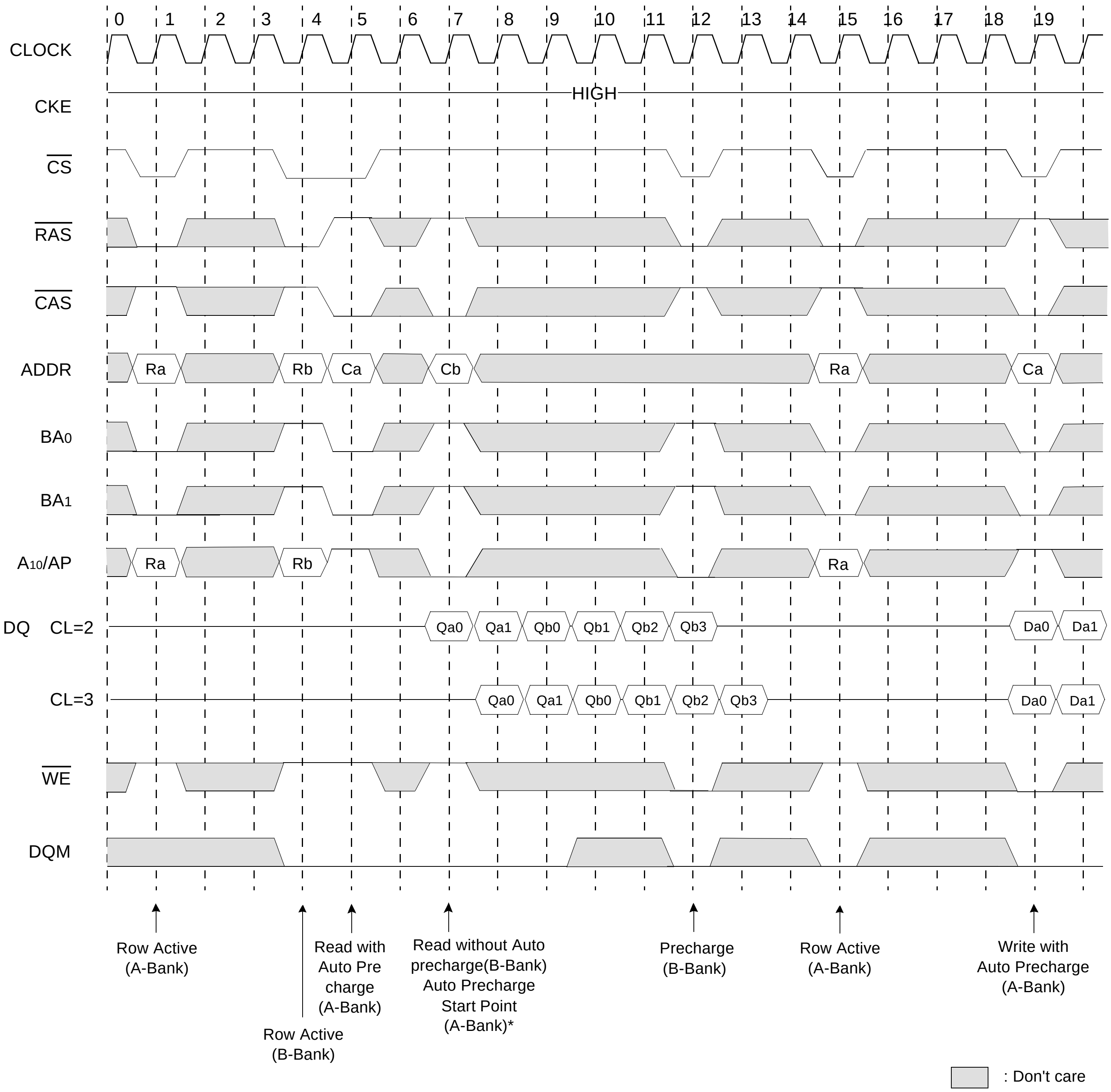
***Note :** 1. tCDL should be met to complete write.

Read & Write Cycle with Auto Precharge I @Burst Length=4



***Note :** 1. t_{RCD} should be controlled to meet minimum t_{RAS} before internal precharge start.
(In the case of Burst Length=1 & 2, BRSW mode and Block write)

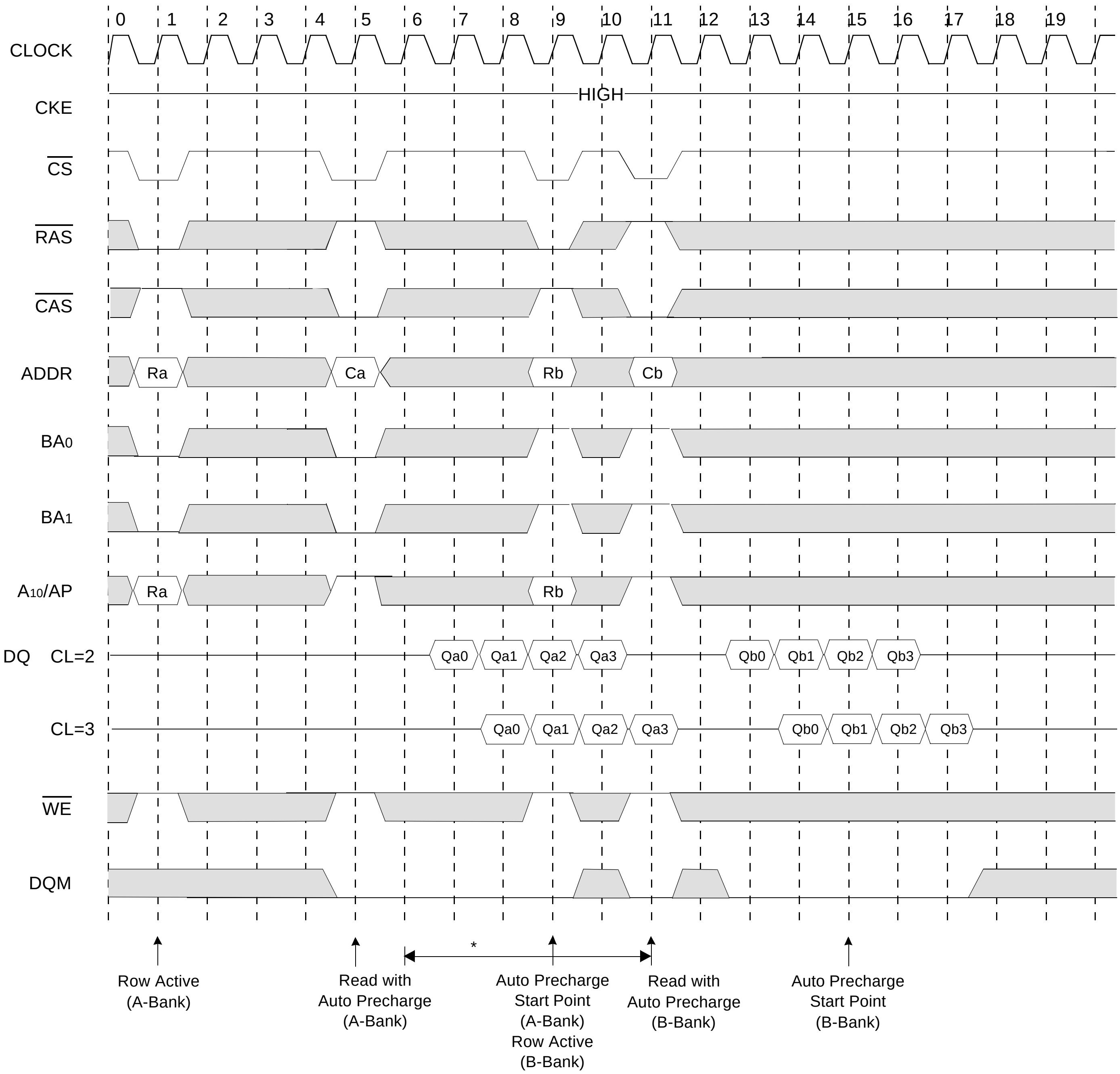
Read & Write Cycle with Auto Precharge II @Burst Length=4



***Note:** * When Read(Write) command with auto precharge is issued at A-Bank after A and B Bank activation.

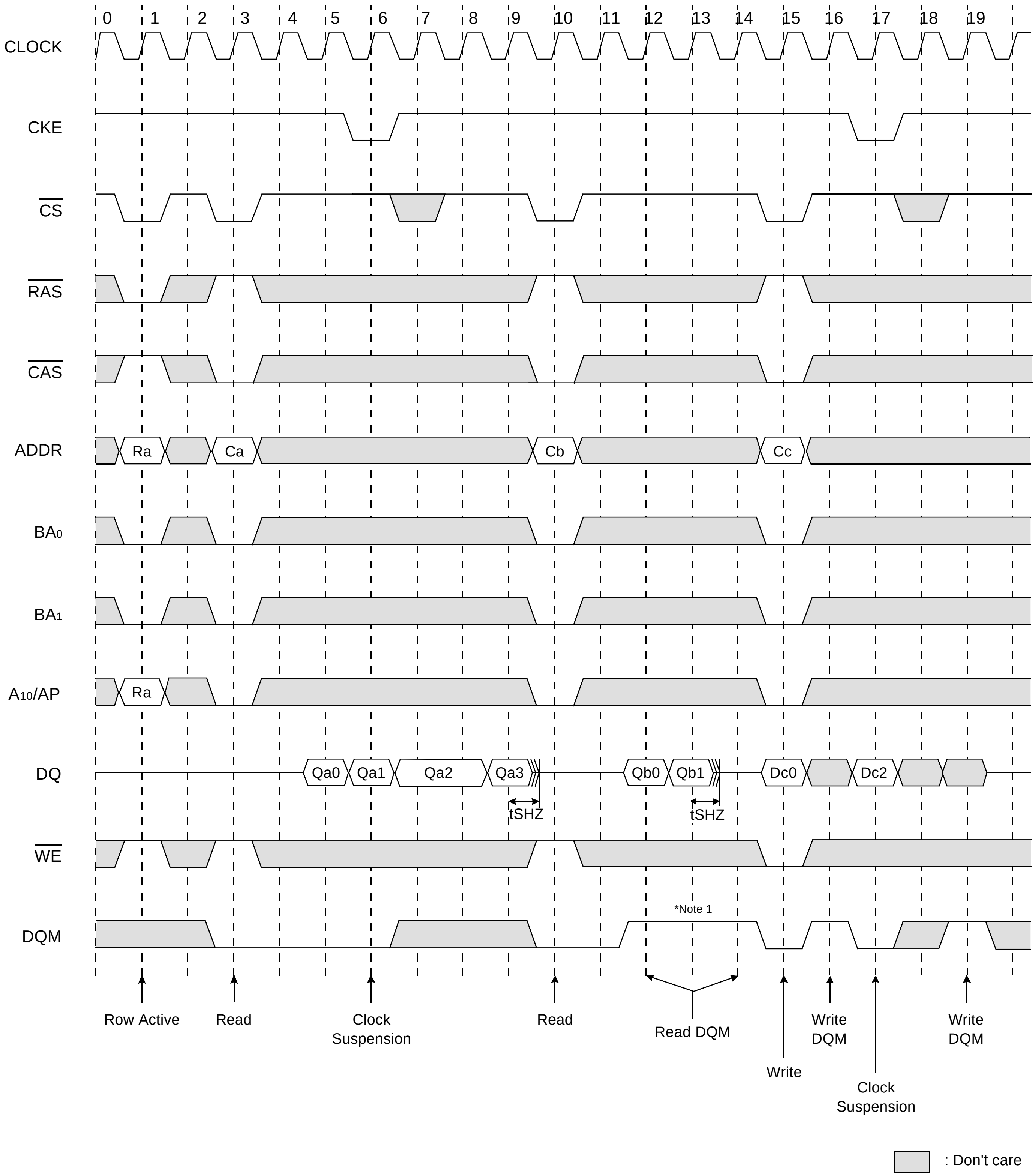
- if Read(Write) command without auto precharge is issued at B-Bank before A Bank auto precharge starts, A Bank auto precharge will start at B Bank read command input point .
- any command can not be issued at A Bank during tRP after A Bank auto precharge starts.

Read & Write Cycle with Auto Precharge III @Burst Length=4



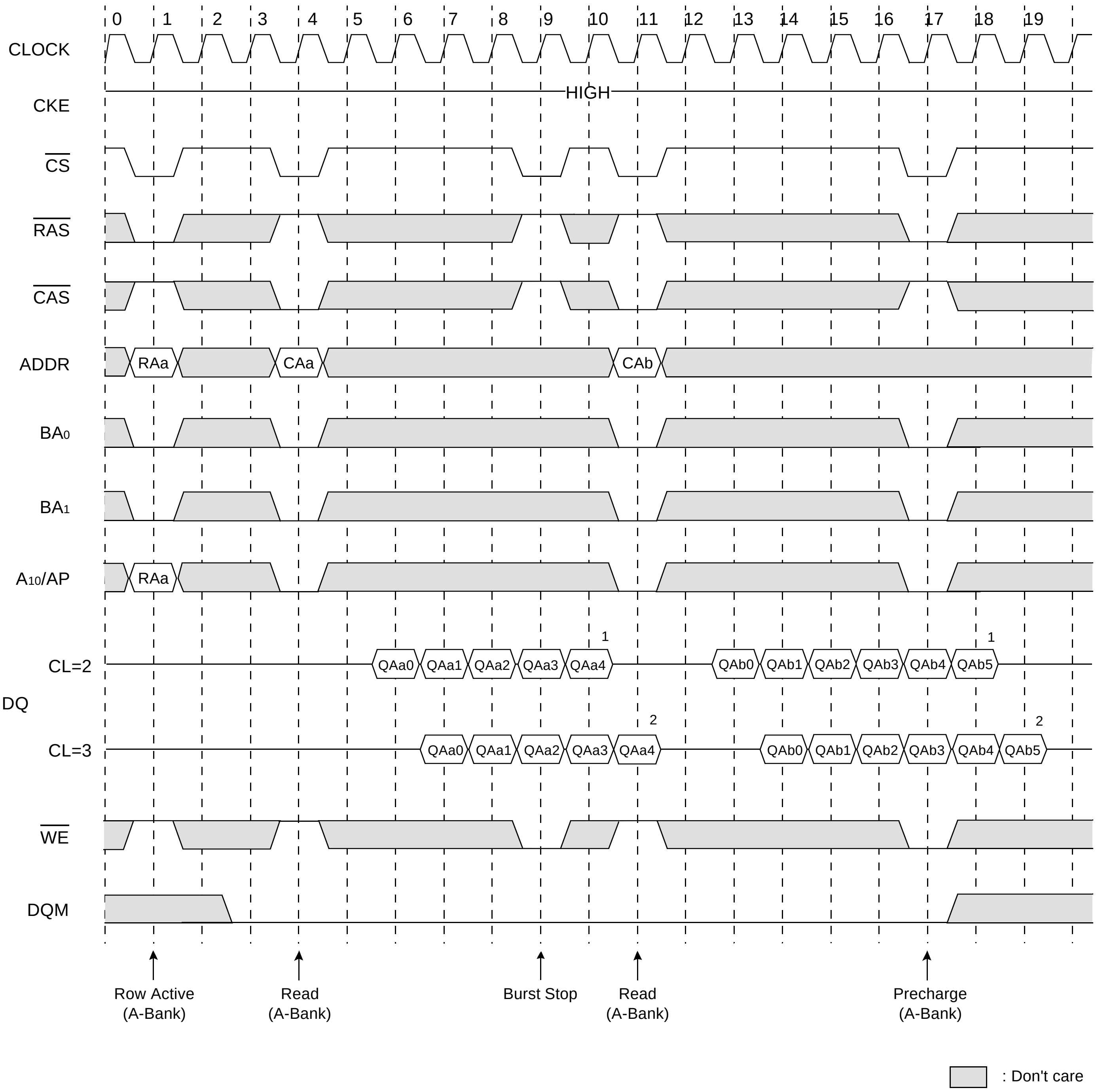
***Note :** * Any command to A-bank is not allowed in this period.
tRP is determined from at auto precharge start point

Clock Suspension & DQM Operation Cycle @CAS Latency=2, Burst Length=4



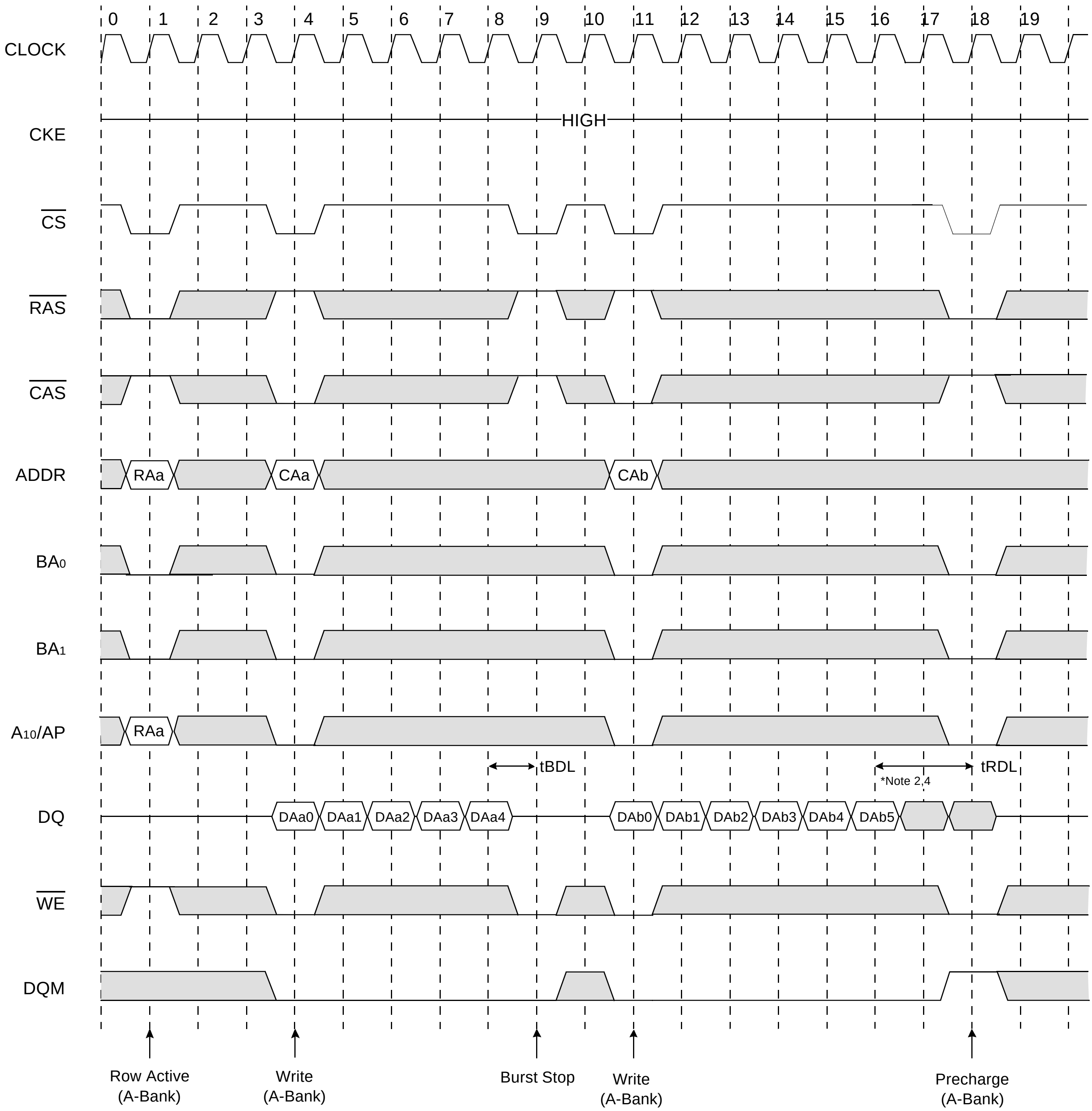
***Note :** 1. DQM is needed to prevent bus contention.

Read Interrupted by Precharge Command & Read Burst Stop Cycle @Burst Length=Full page



***Note :**
1. At full page mode, burst is wrap-around at the end of burst. So auto precharge is impossible.
2. About the valid DQs after burst stop, it is same as the case of RAS interrupt.
   Both cases are illustrated above timing diagram. See the label 1, 2 on them.
   But at burst write, Burst stop and RAS interrupt should be compared carefully.
   Refer the timing diagram of "Full page write burst stop cycle".
3. Burst stop is valid at every burst length.

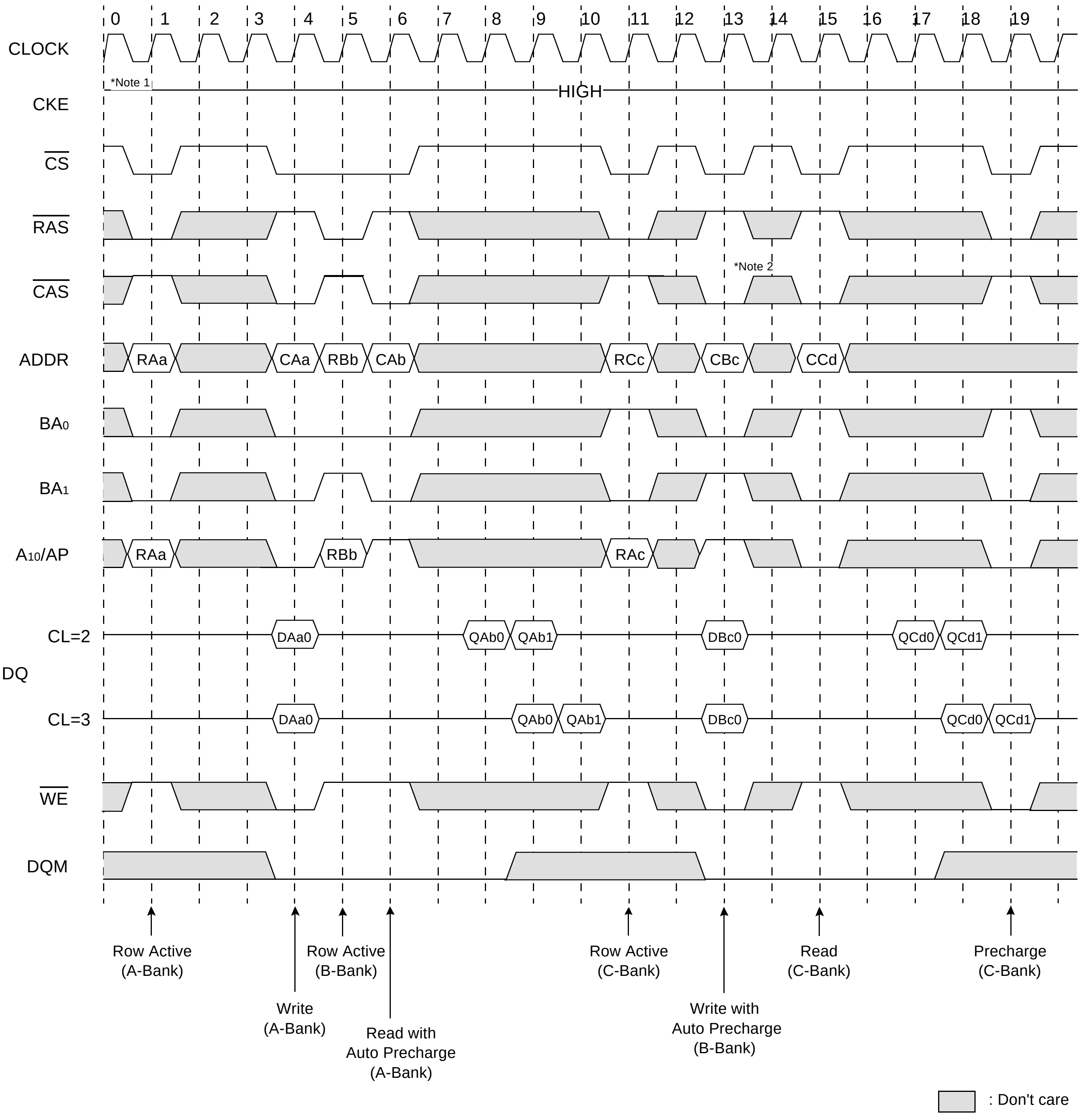
Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Burst Length=Full page



***Note :**

1. At full page mode, burst is wrap-around at the end of burst. So auto precharge is impossible.
2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of tRDL. DQM at write interrupted by precharge command is needed to prevent invalid write.
   DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst.
   Input data after Row precharge cycle will be masked internally.
3. Burst stop is valid at every burst length.
4. For -55/60/70/80/10, tRDL=1CLK product can be supported within restricted amounts and it will be distinguished by bucket code "NV". From the next generation, tRDL will be only 2CLK for every clock frequency.

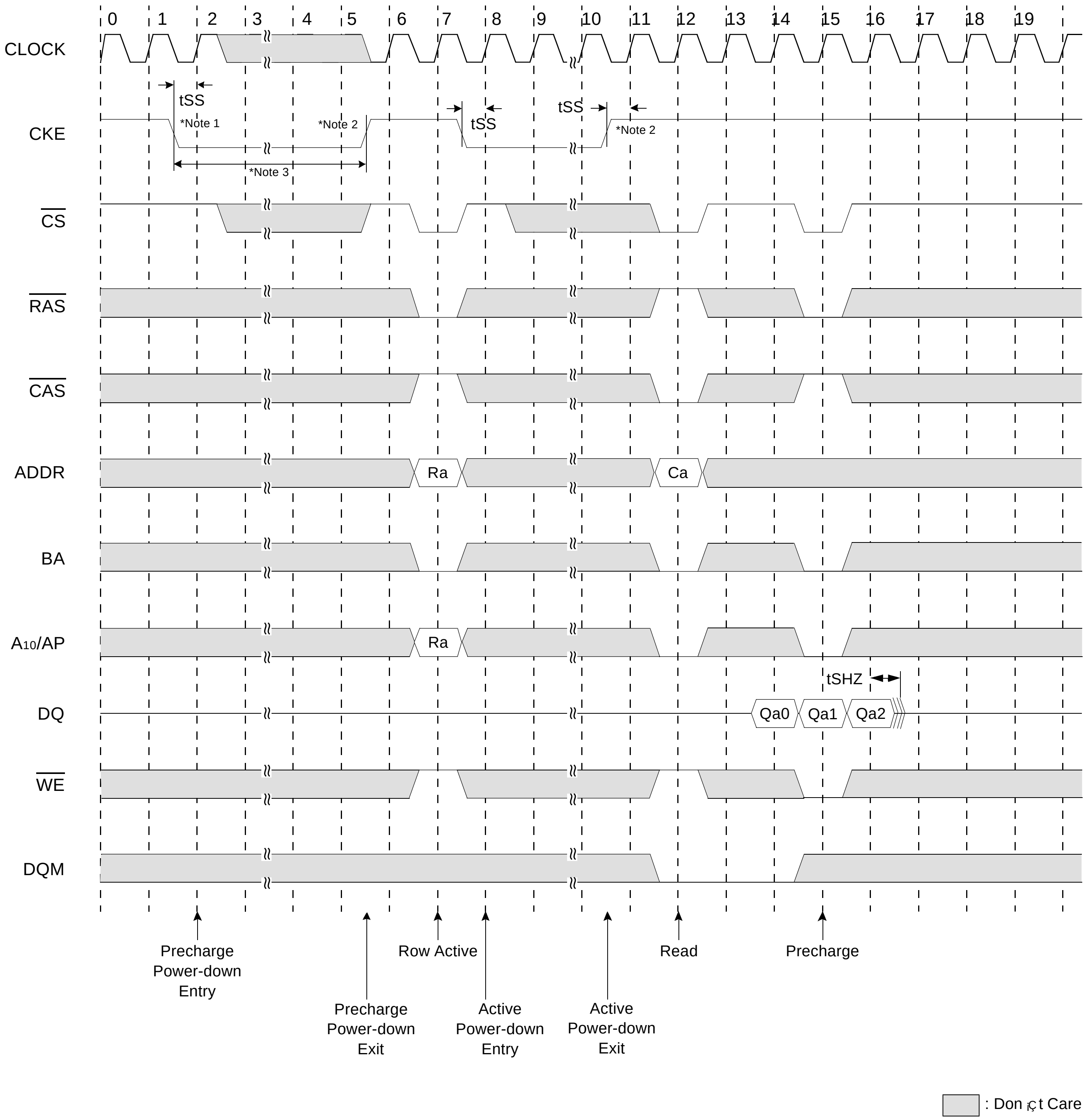
Burst Read Single bit Write Cycle @Burst Length=2



***Note :**

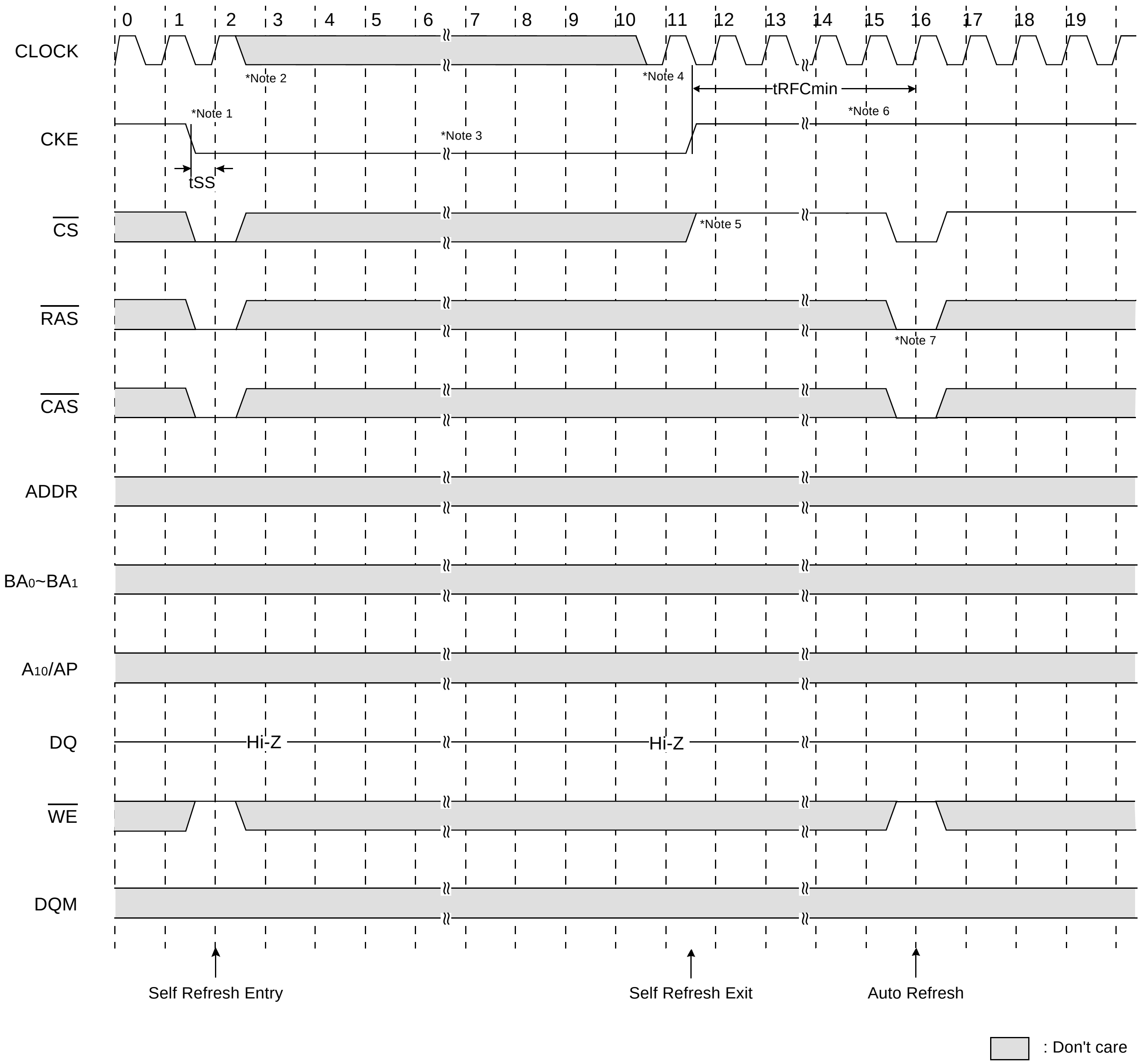
1. BRSW modes is enabled by setting A_9 "High" at MRS (Mode Register Set).
   At the BRSW Mode, the burst length at write is fixed to "1" regardless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.
   Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command, the next cycle starts the precharge.

Active/Precharge Power Down Mode @CAS Latency=2, Burst Length=4



***Note :** 1. Both banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least 1CLK + tss prior to Row active command.
3. Can not violate minimum refresh specification. (64ms)

Self Refresh Entry & Exit Cycle



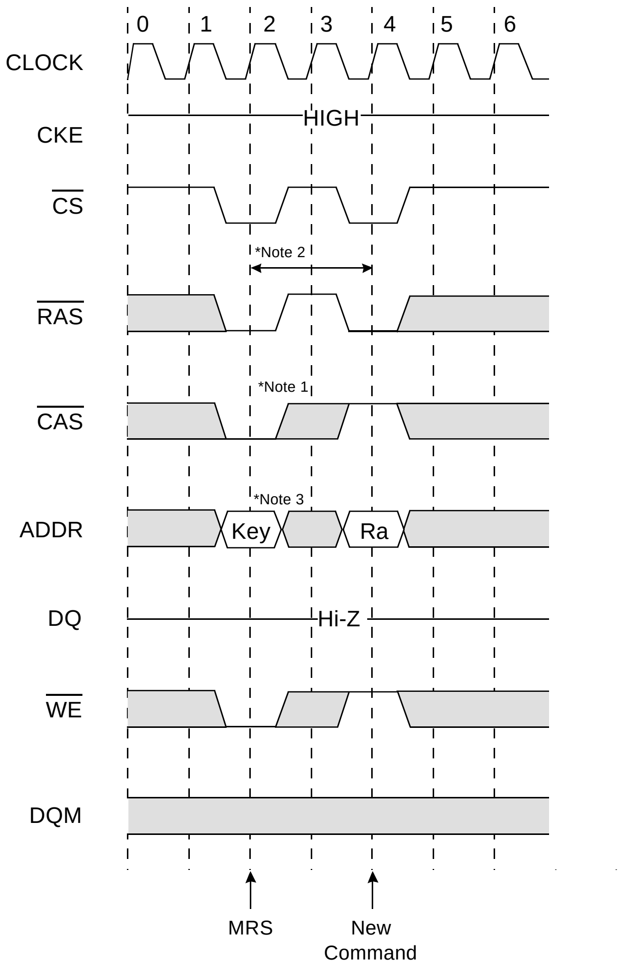
***Note :** **TO ENTER SELF REFRESH MODE**

1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clcok cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low".
   cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

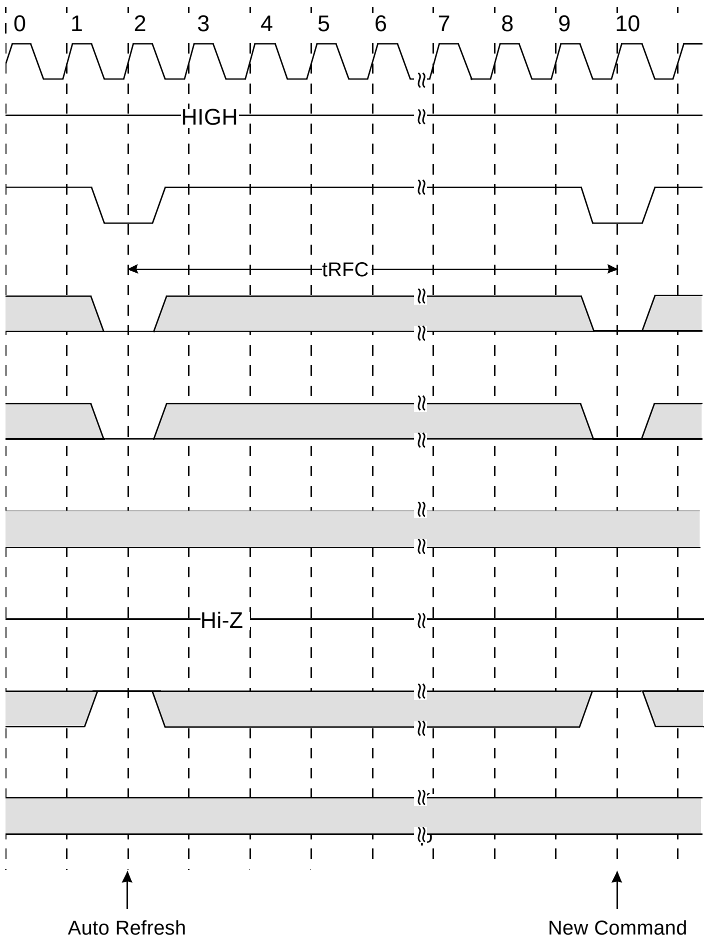
TO EXIT SELF REFRESH MODE

4. System colck restart and be stable before returning CKE high.
5. $\overline{CS}$ starts from high.
6. Minimum t_{RFC} is required after CKE going high to complete self refresh exit.
7. 4K cycle of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

Mode Register Set Cycle



Auto Refresh Cycle



: Don't care

* All banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE

***Note :**
1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, & $\overline{WE}$ activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new $\overline{RAS}$ activation.
3. Please refer to Mode Register Set table.

PACKAGE DIMENSIONS

86-TSOP2-400F

Unit : Millimeters

